Sheng Lin

List of Publications by Year
in descending order

17 papers	**1,003** citations	933447 **10** h-index	1281871 **11** g-index
17 all docs	**17** docs citations	**17** times ranked	**692** citing authors

#	Article	IF	Citations
1	Has the inter-regional transmission expansion promoted the low-carbon transition of China's power sector?. Computers and Industrial Engineering, 2022, 168, 108059.	6.3	16
2	Has the inter-regional transmission grid promoted clean power development? A quantitative assessment on China's electricity sector. Journal of Cleaner Production, 2020, 269, 122370.	9.3	18
3	When Sorting Network Meets Parallel Bitstreams: A Fault-Tolerant Parallel Ternary Neural Network Accelerator based on Stochastic Computing. , 2020, , .		15
4	ResNet Can Be Pruned 60Ã—: Introducing Network Purification and Unused Path Removal (P-RM) after Weight Pruning. , 2019, , .		21
5	Sequestration of Antimonite by Zerovalent Iron: Using Weak Magnetic Field Effects to Enhance Performance and Characterize Reaction Mechanisms. Environmental Science & Technology, 2016, 50, 1483-1491.	10.0	81
6	Enhanced removal efficiency of bromate from aqueous solutions by nanoscale zero-valent iron immobilized on activated carbon. Desalination and Water Treatment, 2015, 54, 2480-2489.	1.0	13
7	Ordered mesoporous carbon immobilized nano zero-valent iron in bromate removal from aqueous solution. Journal of the Taiwan Institute of Chemical Engineers, 2014, 45, 3000-3006.	5.3	25
8	Fast and Highly Efficient Removal of Chromate from Aqueous Solution Using Nanoscale Zero-Valent Iron/Activated Carbon (NZVI/AC). Water, Air, and Soil Pollution, 2014, 225, 1.	2.4	43
9	Bromate removal from aqueous solutions by ordered mesoporous carbon. Environmental Technology (United Kingdom), 2014, 35, 984-992.	2.2	10
10	Design of a Ternary Memory Cell Using CNTFETs. IEEE Nanotechnology Magazine, 2012, 11, 1019-1025.	2.0	116
11	CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits. IEEE Nanotechnology Magazine, 2011, 10, 217-225.	2.0	430
12	A 11-Transistor Nanoscale CMOS Memory Cell for Hardening to Soft Errors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 900-904.	3.1	58
13	Design of a CNTFET-Based SRAM Cell by Dual-Chirality Selection. IEEE Nanotechnology Magazine, 2010, 9, 30-37.	2.0	86
14	A novel design technique for soft error hardening of Nanoscale CMOS memory. , 2009, , .		6
15	A Novel Hardened Design of a CMOS Memory Cell at 32nm. , 2009, , .		4
16	A new SRAM cell design using CNTFETs. , 2008, , .		43
17	A Highly-Stable Nanometer Memory for Low-Power Design. , 2008, , .		18