## Piotr Dudek

## List of Publications by Year in Descending Order

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.



#	Paper	IF	Citations
49	Agile reactive navigation for a non-holonomic mobile robot using a pixel processor array. <i>IET Image Processing</i> , <b>2021</b> , 15, 1883-1892	1.7	O
48	Proximity Estimation Using Vision Features Computed On Sensor <b>2020</b> ,		2
47	Visual Odometry Using Pixel Processor Arrays for Unmanned Aerial Systems in GPS Denied Environments. <i>Frontiers in Robotics and AI</i> , <b>2020</b> , 7, 126	2.8	2
46	Real-Time Depth From Focus on a Programmable Focal Plane Processor. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , <b>2018</b> , 65, 925-934	3.9	7
45	Perspective Correcting Visual Odometry for Agile MAVs using a Pixel Processor Array 2018,		3
44	High-speed depth from focus on a programmable vision chip using a focus tunable lens 2017,		4
43	Visual Odometry for Pixel Processor Arrays <b>2017</b> ,		8
42	Tracking control of a UAV with a parallel visual processor 2017,		10
41	A Demonstration of Tracking using Dynamic Neural Fields on a Programmable Vision Chip <b>2016</b> ,		2
40	Parallel HDR tone mapping and auto-focus on a cellular processor array vision chip 2016,		7
39	Gradient-descent-based learning in memristive crossbar arrays <b>2015</b> ,		15
38	An event-driven massively parallel fine-grained processor array 2015,		1
37	Toward joint approximate inference of visual quantities on cellular processor arrays 2015,		4
36	Practical gradient-descent for memristive crossbars 2015,		1
35	Trigger-Wave Asynchronous Cellular Logic Array for Fast Binary Image Processing. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , <b>2015</b> , 62, 497-506	3.9	1
34	A new method for fast skeletonization of binary images on cellular processor arrays 2014,		3
33	A Fast Self-Tuning Background Subtraction Algorithm <b>2014</b> ,		52

## (2011-2014)

32	Tunable CMOS Delay Gate With Improved Matching Properties. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , <b>2014</b> , 61, 2586-2595	3.9	13
31	The accuracy and scalability of continuous-time Bayesian inference in analogue CMOS circuits 2014,		6
30	Characterization of processing errors on analog fully-programmable cellular sensor-processor arrays <b>2014</b> ,		1
29	Mixed signal SIMD processor array vision chip for real-time image processing. <i>Analog Integrated Circuits and Signal Processing</i> , <b>2013</b> , 77, 385-399	1.2	11
28	A general-purpose vision processor with 160B0 pixel-parallel SIMD processor array 2013,		2
27	AMBER: Adapting multi-resolution background extractor 2013,		4
26	Mixed signal SIMD cellular processor array vision chip operating at 30,000 fps <b>2012</b> ,		2
25	VLSI circuits implementing computational models of neocortical circuits. <i>Journal of Neuroscience Methods</i> , <b>2012</b> , 210, 93-109	3	25
24	A compact FPGA implementation of a bit-serial SIMD cellular processor array 2012,		3
23	Low power multiple object tracking and counting using a SCAMP cellular processor array 2012,		1
22	Coarse grain mapping method for image processing on fine grain cellular processor arrays 2012,		1
21	Trigger-wave collision detecting asynchronous cellular logic array for fast image skeletonization <b>2012</b> ,		5
20	Heterogeneous neurons and plastic synapses in a reconfigurable cortical neural network IC 2012,		1
19	A SIMD Cellular Processor Array Vision Chip With Asynchronous Processing Capabilities. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , <b>2011</b> , 58, 2420-2431	3.9	45
18	Asynchronous cellular logic network as a co-processor for a general-purpose massively parallel array. <i>International Journal of Circuit Theory and Applications</i> , <b>2011</b> , 39, 963-972	2	14
17	Architecture and design of a programmable 3D-integrated cellular processor array for image processing <b>2011</b> ,		2
16	Analogue CMOS circuit implementation of a dopamine modulated synapse 2011,		1
15	A processor element for a mixed signal cellular processor array vision chip <b>2011</b> ,		5

14	An 80B0 general-purpose digital vision chip in 0.18th CMOS technology <b>2010</b> ,	6
13	Autonomous long distance transfer on SIMD cellular processor arrays 2010,	5
12	Hardware Implementation of Skeletonization Algorithm for Parallel Asynchronous Image Processing. <i>Journal of Signal Processing Systems</i> , <b>2009</b> , 56, 91-103	8
11	A CMOS circuit implementation of a spiking neuron with bursting and adaptation on a biological timescale <b>2009</b> ,	12
10	A pixel-parallel cellular processor array in a stacked three-layer 3D silicon-on-insulator technology <b>2009</b> ,	8
9	ASPA: Focal Plane digital processor array with asynchronous processing capabilities 2008,	9
8	Implementing the grayscale wave metric on a cellular array processor chip 2008,	2
7	Integrated circuit implementation of a cortical neuron 2008,	15
7	Integrated circuit implementation of a cortical neuron <b>2008</b> ,  Compact silicon neuron circuit with spiking and bursting behaviour. <i>Neural Networks</i> , <b>2008</b> , 21, 524-34 9.1	15 201
6	Compact silicon neuron circuit with spiking and bursting behaviour. <i>Neural Networks</i> , <b>2008</b> , 21, 524-34 9.1	201
5	Compact silicon neuron circuit with spiking and bursting behaviour. <i>Neural Networks</i> , <b>2008</b> , 21, 524-34 9.1  Evolution of Pixel Level Snakes towards an efficient hardware implementation <b>2007</b> ,	201
5	Compact silicon neuron circuit with spiking and bursting behaviour. <i>Neural Networks</i> , <b>2008</b> , 21, 524-34 9.1  Evolution of Pixel Level Snakes towards an efficient hardware implementation <b>2007</b> ,  Simple Analogue VLSI Circuit of a Cortical Neuron <b>2006</b> ,	201