Chih-Kong Ken Yang

List of Publications by Year
in descending order

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50	1,066	394421	454955
papers	citations	19 h-index	30 g-index

50	50	50	888
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A Scalable 20V Charge-Pump-Based Driver in 65nm CMOS Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 55-59.	3.0	2
2	A 6Î¼m-Precision Pulsed-Coherent Lidar with a 40-dB Tuning Range Inverter-Based Phase-Invariant PGA. , 2021, , .		1
3	A 25Gb/s 185mW PAM-4 Receiver with 4-Tap Adaptive DFE and Sampling Clock Optimization in 55nm CMOS. , 2021, , .		0
4	A 9-Î¼m Precision 5-MSa/s Pulsed-Coherent Lidar System With Subsampling Receiver. IEEE Solid-State Circuits Letters, 2020, 3, 262-265.	2.0	11
5	A 19-GHz Pulsed-Coherent ToF Receiver With 40-Î¼m Precision for Laser Ranging Systems. , 2019, , .		1
6	A 19-GHz Pulsed-Coherent ToF Receiver With 40-mu m Precision for Laser Ranging Systems. IEEE Solid-State Circuits Letters, 2019, 2, 191-194.	2.0	3
7	A 36-V 49% Efficient Hybrid Charge Pump in Nanometer-Scale Bulk CMOS Technology. IEEE Journal of Solid-State Circuits, 2017, 52, 781-798.	5.4	23
8	A 32â€“48 Gb/s Serializing Transmitter Using Multiphase Serialization in 65 nm CMOS Technology. IEEE Journal of Solid-State Circuits, 2015, 50, 763-775.	5.4	87
9	A 50â€“64 Gb/s Serializing Transmitter With a 4-Tap, LC-Ladder-Filter-Based FFE in 65 nm CMOS Technology. IEEE Journal of Solid-State Circuits, 2015, 50, 1903-1916.	5.4	39
10	A 12-V charge pump-based square wave driver in 65-nm CMOS technology. , 2014, , .		8
11	A compact stacked-device output driver in low-voltage CMOS Technology. , 2014, , .		8
12	Flexible-Assignment Calibration Technique for Mismatch-Constrained Digital-to-Analog Converters. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1934-1944.	3.1	11
13	Reference Calibration of Body-Voltage Sensing Circuit for High-Speed STT-RAMs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2932-2939.	5.4	19
14	A 100+ Meter 12 Gb/s/Lane Copper Cable Link Based on Clock-Forwarding. IEEE Journal of Solid-State Circuits, 2013, 48, 1085-1098.	5.4	3
15	Electrostatic bottom-driven rotary stage on multiple conductive liquid-ring bearings. , 2013, , .		2
16	A 32-to-48Gb/s serializing transmitter using multiphase sampling in 65nm CMOS. , 2013, , .		21
17	Analysis and Design of Superharmonic Injection-Locked Multipath Ring Oscillators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 1712-1725.	5.4	11
18	A 0.1â€“1.5 GHz 8-bit Inverter-Based Digital-to-Phase Converter Using Harmonic Rejection. IEEE Journal of Solid-State Circuits, 2013, 48, 2681-2692.	5.4	42

#	Article	IF	Citations
19	A multi-phase multi-frequency clock generator using superharmonic injection locked multipath ring oscillators as frequency dividers. , 2012, , .		3
20	A low-power highly multiplexed parallel PRBS generator. , 2012, , .		9
21	Power Optimized ADC-Based Serial Link Receiver. IEEE Journal of Solid-State Circuits, 2012, 47, 938-951.	5.4	46
22	Scalability and Design-Space Analysis of a 1T-1MTJ Memory Cell for STT-RAMs. IEEE Transactions on Electron Devices, 2012, 59, 878-887.	3.0	73
23	Design and Optimization of Multipath Ring Oscillators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2332-2345.	5.4	31
24	Multilevel Power Optimization of Pipelined A/D Converters. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 832-845.	3.1	18
25	Circuit-Level Performance Evaluation of Schottky Tunneling Transistor in Mixed-Signal Applications. IEEE Nanotechnology Magazine, 2011, 10, 291-299.	2.0	10
26	Equalizer Design and Performance Trade-Offs in ADC-Based Serial Links. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2096-2107.	5.4	32
27	Guest Editorial for Special Issue on High-Performance Multichip Interconnections. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 317-318.	3.0	0
28	ADC-Based Serial I/O Receivers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2248-2258.	5.4	27
29	A Phase-Selecting Digital Phase-Locked Loop With Bandwidth Tracking in 65-nm CMOS Technology. IEEE Journal of Solid-State Circuits, 2010, 45, 781-792.	5.4	14
30	Convex Piecewise-Linear Modeling Method for Circuit Optimization via Geometric Programming. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1823-1827.	2.7	21
31	A nonlinear phase detector for digital phase locked loops. , 2009, , .		2
32	ADC-based serial I/O receivers. , 2009, , .		8
33	An LC-Based Clock Buffer With Tunable Injection Locking. IEEE Journal of Solid-State Circuits, 2009, 44, 797-807.	5.4	3
34	A 4.8 GS/s 5-bit ADC-Based Receiver With Embedded DFE for Signal Equalization. IEEE Journal of Solid-State Circuits, 2009, 44, 901-915.	5.4	30
35	Minimizing the Supply Sensitivity of a CMOS Ring Oscillator Through Jointly Biasing the Supply and Control Voltages. IEEE Journal of Solid-State Circuits, 2009, 44, 2488-2495.	5.4	28
36	A Comprehensive Delay Model for CMOS CML Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 2608-2618.	5.4	30

#	Article	IF	Citations
37	Near-Optimal Equalizer and Timing Adaptation for I/O Links Using a BER-Based Metric. IEEE Journal of Solid-State Circuits, 2008, 43, 2144-2156.	5.4	34
38	Edge and Data Adaptive Equalization of Serial-Link Transceivers. IEEE Journal of Solid-State Circuits, 2008, 43, 2157-2169.	5.4	35
39	Phase correction of a resonant clocking system using resonant interpolators. , 2008, , .		5
40	Technique to Reduce the Resolution Requirement of Digitally Controlled Oscillators for Digital PLLs. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 237-241.	2.2	8
41	A 5-mW 6-Gb/s Quarter-Rate Sampling Receiver With a 2-Tap DFE Using Soft Decisions. IEEE Journal of Solid-State Circuits, 2007, 42, 881-888.	5.4	54
42	BER-based Adaptation of I/O Link Equalizers. , 2007, , .		2
43	Precursor ISI Reduction in High-Speed I/O. , 2007, , .		17
44	Device-circuit co-optimization for mixed-mode circuit design via geometric programming. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	0
45	Modified LMS Adaptation Algorithm for a Discrete-Time Edge Equalizer of Serial I/O. , 2006, , .		8
46	A Study of the Optimal Data Rate for Minimum Power of I/Os. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 1230-1234.	2.2	10
47	Methodology for on-chip adaptive jitter minimization in phase-locked loops. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2003, 50, 870-878.	2.2	20
48	A low-power adaptive bandwidth PLL and clock buffer with supply-noise compensation. IEEE Journal of Solid-State Circuits, 2003, 38, 1804-1812.	5.4	94
49	A 0.8-Î¼m CMOS 2.5 Gb/s oversampling receiver and transmitter for serial links. IEEE Journal of Solid-State Circuits, 1996, 31, 2015-2023.	5.4	79
50	Techniques for improving the accuracy of geometric-programming based analog circuit design optimization. , 0, , .		23