Shreepad Panth

List of Publications by Year
in descending order

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14 papers	300 citations	1937685 4 h-index	2272923 4 g-index
14 all docs	14 docs citations	14 times ranked	225 citing authors

#	Article	IF	Citations
1	Adaptive Regression-Based Thermal Modeling and Optimization for Monolithic 3-D ICs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1707-1720.	2.7	18
2	Placement-Driven Partitioning for Congestion Mitigation in Monolithic 3D IC Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 540-553.	2.7	48
3	Evaluating Chip-Level Impact of Cu/Low-<inline-formula> <tex-math notation="LaTeX">$kappa $ </tex-math></inline-formula> Performance Degradation on Circuit Performance at Future Technology Nodes. IEEE Transactions on Electron Devices, 2015, 62, 940-946.	3.0	12
4	Design and Analysis of 3D-MAPS (3D Massively Parallel Processor with Stacked Memory). IEEE Transactions on Computers, 2015, 64, 112-125.	3.4	52
5	Design challenges and solutions for ultra-high-density monolithic 3D ICs. , 2014, , .		39
6	Impact of size effects in local interconnects for future technology nodes: A study based on full-chip layouts. , 2014, , .		23
7	High-density integration of functional modules using monolithic 3D-IC technology. , 2013, , .		52
8	Test-TSV estimation during 3D-IC partitioning. , 2013, , .		1
9	TSV Stress-Aware ATPG for 3D Stacked ICs. , 2012, , .		9
10	Scan test of die logic in 3D ICs using TSV probing. , 2012, , .		10
11	Transition delay fault testing of 3D ICs with IR-drop study. , 2012, , .		4
12	A study of TSV variation impact on power supply noise. , 2011, , .		7
13	Designing 3D test wrappers for pre-bond and post-bond test of 3D embedded cores. , 2011, , .		15
14	Scan chain and power delivery network synthesis for pre-bond test of 3D ICs. , 2011, , .		10