Charles Augustine

List of Publications by Year
in descending order

23 papers	801 citations	1040056 9 h-index	1372567 10 g-index
23 all docs	23 docs citations	23 times ranked	745 citing authors

#	Article	IF	Citations
1	Spin-Based Neuron Model With Domain-Wall Magnets as Synapse. IEEE Nanotechnology Magazine, 2012, 11, 843-853.	2.0	154
2	KNACK: A hybrid spin-charge mixed-mode simulator for evaluating different genres of spin-transfer torque MRAM bit-cells. , 2011, , .		118
3	Modeling of failure probability and statistical design of spin-torque transfer magnetic random access memory (STT MRAM) array for yield enhancement. , 2008, , .		72
4	Physics-Based SPICE-Compatible Compact Model for Simulating Hybrid MTJ/CMOS Circuits. IEEE Transactions on Electron Devices, 2013, 60, 2808-2814.	3.0	70
5	Low-power functionality enhanced computation architecture using spin-based devices. , 2011, , .		56
6	Enabling Wide Autonomous DVFS in a 22 nm Graphics Execution Core Using a Digitally Controlled Fully Integrated Voltage Regulator. IEEE Journal of Solid-State Circuits, 2016, 51, 18-30.	5.4	54
7	Spin-Transfer Torque MRAMs for Low Power Memories: Perspective and Prospective. IEEE Sensors Journal, 2012, 12, 756-766.	4.7	40
8	Effect of quantum confinement on spin transport and magnetization dynamics in dual barrier spin transfer torque magnetic tunnel junctions. Journal of Applied Physics, 2010, 108, .	2.5	39
9	Boolean and non-Boolean computation with spin devices. , 2012, , .		33
10	A Variation-Adaptive Integrated Computational Digital LDO in 22-nm CMOS With Fast Transient Response. IEEE Journal of Solid-State Circuits, 2020, 55, 977-987.	5.4	27
11	Ultra-Low Power Nanomagnet-Based Computing: A System-Level Perspective. IEEE Nanotechnology Magazine, 2011, 10, 778-788.	2.0	26
12	Ultra low energy analog image processing using spin based neurons. , 2012, , .		20
13	STT-MRAMs for future universal memories: Perspective and prospective. , 2012, , .		18
14	An Energy-Efficient Graphics Processor in 14-nm Tri-Gate CMOS Featuring Integrated Voltage Regulators for Fine-Grain DVFS, Retentive Sleep, and <inline-formula> <tex-math notation="LaTeX">${V}_{ext{MIN}}$ </tex-math> </inline-formula> Optimization. IEEE Journal of Solid-State Circuits, 2019, 54, 144-157.	5.4	17
15	A design methodology and device/circuit/architecture compatible simulation framework for low-power Magnetic Quantum Cellular Automata systems. , 2009, , .		16
16	Energy efficient many-core processor for recognition and mining using spin-based memory. , 2011, , .		12
17	PETE: A device/circuit analysis framework for evaluation and comparison of charge based emerging devices. , 2009, , .		11
18	Nano Spiral Inductors for Low-Power Digital Spintronic Circuits. IEEE Transactions on Magnetics, 2010, 46, 1898-1901.	2.1	9

#	Article	IF	Citations
19	Dual pillar spin-transfer torque MRAMs for low power applications. ACM Journal on Emerging Technologies in Computing Systems, 2013, 9, 1-17.	2.3	6
20	Spin torques estimation and magnetization dynamics in dual barrier resonant tunneling penta-layer magnetic tunnel junctions. , 2010, , .		2
21	Realistic spin-FET performance assessment for reconfigurable logic circuits. , 2010, , .		1
22	Self-Consistent Transport-Magnetic Simulation and Benchmarking of Hybrid Spin-Torque Driven Magnetic Tunnel Junctions (MTJs). , 2010, , .		0
23	Dual ferroelectric capacitor architecture and its application to TAG RAM. , 2010, , .		0