Zainalabedin Navabi

List of Publications by Year in Descending Order

62 papers	214 citations	6 h-index	10 g-index
94 ext. papers	307 ext. citations	1.7 avg, IF	2.99 L-index

#	Paper	IF	Citations
62	DiBA: n-Dimensional Bitslice Architecture for LSTM Implementation **2020**,		1
61	LUT Input Reordering to Reduce Aging Impact on FPGA LUTs. *IEEE Transactions on Computers*, **2020**, 69, 1500-1506	2.5	1
60	Automatic Correction of Dynamic Power Management Architecture in Modern Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 308-318	2.6	1
59	Near-Optimal Node Selection Procedure for Aging Monitor Placement **2018**,		1
58	Scalable Symbolic Simulation-Based Automatic Correction of Modern Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 1845-1853	2.6	
57	TruncApp: A truncation-based approximate divider for energy efficient DSP applications **2017**,		20
56	Bridging Presilicon and Postsilicon Debugging by Instruction-Based Trace Signal Selection in Modern Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2059-2070	2.6	2
55	Reducing Search Space for Fault Diagnosis: A Probability-Based Scoring Approach **2017**,		3
54	SENSIBle: A Highly Scalable SENsor DeSIgn for Path-Based Age Monitoring in FPGAs. *IEEE Transactions on Computers*, **2017**, 66, 919-926	2.5	14
53	A novel SAT-based ATPG approach for transition delay faults **2017**,		2
52	Stochastic testing of processing cores in a many-core architecture. *The Integration VLSI Journal*, **2016**, 55, 183-193	1.4	3
51	Self-Healing Many-Core Architecture: Analysis and Evaluation. *VLSI Design*, **2016**, 2016, 1-17		2
50	An improved scheme for pre-computed patterns in core-based SoC architecture **2016**,		3
49	Early prediction of timing critical instructions in pipeline processor **2016**,		1
48	Multi-valued logic test access mechanism for test time and power reduction **2015**,		2
47	System-level assertions: approach for electronic system-level verification. *IET Computers and Digital Techniques*, **2015**, 9, 142-152	0.9	2
46	Low power scheduling in high-level synthesis using dual-Vth library **2015**,		2

45	Aging in digital circuits and age monitoring: Object-oriented modeling and evaluation **2015**,		2
44	Signature oriented model pruning to facilitate multi-threaded processors debugging **2015**,		2
43	Power-aware online testing of manycore systems in the dark silicon era **2015**,		2
42	Hardware Acceleration of Online Error Detection in Many-Core Processors. *Canadian Journal of Electrical and Computer Engineering*, **2015**, 38, 143-153	1.4	4
41	Accelerated On-chip Communication Test Methodology Using a Novel High-Level Fault Model **2015**,		2
40	An off-line MDSI interconnect BIST incorporated in BS 1149.1 **2014**,		2
39	Automatic correction of certain design errors using mutation technique **2014**,		5
38	Improving polynomial datapath debugging with HEDs **2014**,		2
37	Assertion-based verification for system-level designs **2014**,		11
36	A Novel Modeling Approach for System-Level Application Mapping Targeted for Configurable Architecture. *Canadian Journal of Electrical and Computer Engineering*, **2014**, 37, 192-202	1.4	1
35	A probabilistic approach for counterexample generation to aid design debugging **2013**,		3
34	Online periodic test mechanism for homogeneous many-core processors **2013**,		3
33	A new structure for interconnect offline testing **2013**,		1
32	BS 1149.1 extensions for an online interconnect fault detection and recovery **2012**,		3
31	BILBO-friendly hybrid BIST architecture with asymmetric polynomial reseeding **2012**,		3
30	Effective RT-level software-based self-testing of embedded processor cores **2012**,		2
29	A reconfigurable online BIST for combinational hardware using digital neural networks **2010**,		1
28	A partitioning approach to improve reconfigurable neuron-inspired online BIST **2010**,		1

27	Virtual tester development using HDL/PLI **2010**,		3
26	Merit based directed random test generation (MDRTG) scheme for combinational circuits **2010**,		2
25	A mixed HDL/PLI test package **2010**,		5
24	Code optimization for enhancing SystemC simulation time **2010**,		1
23	Optimizing Parametric BIST Using Bio-inspired Computing Algorithms **2009**,		3
22	Stall Power Reduction in Pipelined Architecture Processors **2008**,		1
21	BARP-A Dynamic Routing Protocol for Balanced Distribution of Traffic in NoCs **2008**,		5
20	Reliability in Application Specific Mesh-Based NoC Architectures **2008**,		19
19	An NoC Test Strategy Based on Flooding with Power, Test Time and Coverage Considerations **2008**,		3
18	Utilizing HDL simulation engines for accelerating design and test processes **2008**,		4
17	Reliable NoC architecture utilizing a robust rerouting algorithm **2008**,		3
16	Application specific configuration of a fault-tolerant NoC architecture **2008**,		2
15	A low-power high-throughput link splitting router for NoCs. *Journal of Zhejiang University: Science A* , **2008**, 9, 1708-1714	2.1	1
14	On-Chip Verification of NoCs Using Assertion Processors **2007**,		2
13	Test access to deeply embedded analog terminals within an A/MS SoC. *Journal of Zhejiang University: Science A*, **2007**, 8, 1543-1552	2.1	
12	A New Approach for Design and Verification of Transaction Level Models **2007**,		4
11	An HDL-Based Platform for High Level NoC Switch Testing **2007**,		7
10	Degradable mesh-based on-chip networks using programmable routing tables. *IEICE Electronics Express*, **2007**, 4, 332-339	0.5	5

9	A Test Approach for Look-Up Table Based FPGAs. *Journal of Computer Science and Technology*, **2006** , 21, 141-146	1.7	3
8	A Mesochronous Technique for Communication in Network on Chips **2006**,		1
7	Serial Bus Encoding for Low Power Application **2006**,		4
6	An Optimum ORA BIST for Multiple Fault FPGA Look-Up Table Testing. *Proceedings of the Asian Test Symposium*, **2006**,		4
5	Low-latency Multi-Level Mesh Topology for NoCs **2006**,		5
4	Using RT Level Component Descriptions for Single Stuck-at Hierarchical Fault Simulation. *Journal of Electronic Testing: Theory and Applications (JETTA)*, **2004**, 20, 575-589	0.7	5
3	Compiling gate RC models into a top level simulation model for rough timing analysis of VLSI circuits. *Microprocessors and Microsystems*, **1991**, 15, 313-320	2.4	
2	Compiling an RT level hardware description language into layout of NMOS cells. *Microprocessing and Microprogramming*, **1986**, 18, 123-129		0
1	Generating gate level two phase dynamic MOS logic from AHPL. *Microprocessing and Microprogramming*, **1985**, 16, 89-94		2