Zainalabedin Navabi

List of Publications by Year
in descending order

94 papers	365 citations	1937685 4 h-index	1588992 8 g-index
94 all docs	94 docs citations	94 times ranked	232 citing authors

#	Article	IF	Citations
1	TruncApp: A truncation-based approximate divider for energy efficient DSP applications. , 2017, , .		33
2	Reliability in Application Specific Mesh-Based NoC Architectures. , 2008, , .		26
3	SENSIBle: A Highly Scalable SENsor DeSIgn for Path-Based Age Monitoring in FPGAs. IEEE Transactions on Computers, 2017, 66, 919-926.	3.4	21
4	BARP-A Dynamic Routing Protocol for Balanced Distribution of Traffic in NoCs. , 2008, , .		20
5	Assertion-based verification for system-level designs. , 2014, , .		14
6	A Probabilistic and Constraint Based Approach for Low Power Test Generation. , 2012, , .		11
7	A mixed HDL/PLI test package. , 2010, , .		10
8	Using RT Level Component Descriptions for Single Stuck-at Hierarchical Fault Simulation. Journal of Electronic Testing: Theory and Applications (JETTA), 2004, 20, 575-589.	1.2	8
9	Low-latency Multi-Level Mesh Topology for NoCs. , 2006, , .		8
10	An HDL-Based Platform for High Level NoC Switch Testing. , 2007, , .		8
11	Online Profiling for cluster-specific variable rate refreshing in high-density DRAM systems. , 2017, , .		7
12	An Optimum ORA BIST for Multiple Fault FPGA Look-Up Table Testing. Proceedings of the Asian Test Symposium, 2006, , .	0.0	6
13	A New Approach for Design and Verification of Transaction Level Models. , 2007, , .		6
14	Degradable mesh-based on-chip networks using programmable routing tables. IEICE Electronics Express, 2007, 4, 332-339.	0.8	6
15	BS 1149.1 extensions for an online interconnect fault detection and recovery. , 2012, , .		6
16	A Test Approach for Look-Up Table Based FPGAs. Journal of Computer Science and Technology, 2006, 21, 141-146.	1.5	5
17	Serial Bus Encoding for Low Power Application. , 2006, , .		5
18	An NoC Test Strategy Based on Flooding with Power, Test Time and Coverage Considerations. , 2008, , .		5

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19	Utilizing HDL simulation engines for accelerating design and test processes. , 2008, , .		5
20	Optimizing Parametric BIST Using Bio-inspired Computing Algorithms. , 2009, , .		5
21	Code optimization for enhancing SystemC simulation time. , 2010, , .		5
22	BILBO-friendly hybrid BIST architecture with asymmetric polynomial reseeding. , 2012, , .		5
23	Effective RT-level software-based self-testing of embedded processor cores. , 2012, , .		5
24	An off-line MDSI interconnect BIST incorporated in BS 1149.1. , 2014, , .		5
25	Automatic correction of certain design errors using mutation technique. , 2014, , .		5
26	Back-annotation of Interconnect Physical Properties for System-Level Crosstalk Modeling. , 2019, , .		5
27	LUT Input Reordering to Reduce Aging Impact on FPGA LUTs. IEEE Transactions on Computers, 2020, 69, 1500-1506.	3.4	5
28	Generating gate level two phase dynamic MOS logic from AHPL. Microprocessing and Microprogramming, 1985, 16, 89-94.	0.2	4
29	Reliable NoC architecture utilizing a robust rerouting algorithm. , 2008, , .		4
30	Virtual tester development using HDL/PLI. , 2010, , .		4
31	Mapping Transaction Level Faults to Stuck-At Faults in Communication Hardware. , 2011, , .		4
32	A probabilistic approach for counterexample generation to aid design debugging. , 2013, , .		4
33	Hardware Acceleration of Online Error Detection in Many-Core Processors. Canadian Journal of Electrical and Computer Engineering, 2015, 38, 143-153.	2.0	4
34	Stochastic testing of processing cores in a many-core architecture. The Integration VLSI Journal, 2016, 55, 183-193.	2.1	4
35	DiBA: n-Dimensional Bitslice Architecture for LSTM Implementation. , 2020, , .		4
36	Stall Power Reduction in Pipelined Architecture Processors. , 2008, , .		3

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37	Application specific configuration of a fault-tolerant NoC architecture. , 2008, , .		3
38	A reconfigurable online BIST for combinational hardware using digital neural networks. , 2010, , .		3
39	Polynomial datapath synthesis and optimization based on vanishing polynomial over Z<inf>2</inf>^m and algebraic techniques. , 2012, , .		3
40	Online periodic test mechanism for homogeneous many-core processors. , 2013, , .		3
41	Low power scheduling in high-level synthesis using dual-V<inf>th</inf> library. , 2015, , .		3
42	An improved scheme for pre-computed patterns in core-based SoC architecture. , 2016, , .		3
43	Bridging Presilicon and Postsilicon Debugging by Instruction-Based Trace Signal Selection in Modern Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2059-2070.	3.1	3
44	Reducing Search Space for Fault Diagnosis: A Probability-Based Scoring Approach. , 2017, , .		3
45	An ESL Environment for Modeling Electrical Interconnect Faults. , 2019, , .		3
46	Testing a RISCV-Like Architecture With an HDL-Based Virtual Tester. , 2021, , .		3
47	AFTAB: A RISC-V Implementation with Configurable Gateways for Security. , 2021, , .		3
48	A Mesochronous Technique for Communication in Network on Chips. , 2006, , .		2
49	On-Chip Verification of NoCs Using Assertion Processors. , 2007, , .		2
50	Near optimal machine learning based random test generation. , 2010, , .		2
51	Merit based directed random test generation (MDRTG) scheme for combinational circuits. , 2010, , .		2
52	A new structure for interconnect offline testing. , 2013, , .		2
53	Homogeneous many-core processor system test distribution and execution mechanism. , 2014, , .		2
54	RTL datapath optimization using system-level transformations. , 2014, , .		2

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55	Improving polynomial datapath debugging with HEDs. , 2014, , .		2
56	Power-Aware Online Testing of Manycore Systems in the Dark Silicon Era. , 2015, , .		2
57	Accelerated On-chip Communication Test Methodology Using a Novel High-Level Fault Model. , 2015, , .		2
58	Multi-valued logic test access mechanism for test time and power reduction. , 2015, , .		2
59	Systemâ€level assertions: approach for electronic systemâ€level verification. IET Computers and Digital Techniques, 2015, 9, 142-152.	1.2	2
60	Aging in digital circuits and age monitoring: Object-oriented modeling and evaluation. , 2015, , .		2
61	Signature oriented model pruning to facilitate multi-threaded processors debugging. , 2015, , .		2
62	Self-Healing Many-Core Architecture: Analysis and Evaluation. VLSI Design, 2016, 2016, 1-17.	0.5	2
63	A novel SAT-based ATPG approach for transition delay faults. , 2017, , .		2
64	Automatic Correction of Dynamic Power Management Architecture in Modern Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 308-318.	3.1	2
65	Near-Optimal Node Selection Procedure for Aging Monitor Placement. , 2018, , .		2
66	Built-In Predictors for Dynamic Crosstalk Avoidance. , 2020, , .		2
67	Compiling an RT level hardware description language into layout of NMOS cells. Microprocessing and Microprogramming, 1986, 18, 123-129.	0.2	1
68	Test access to deeply embedded analog terminals within an A/MS SoC. Journal of Zhejiang University: Science A, 2007, 8, 1543-1552.	2.4	1
69	A low-power high-throughput link splitting router for NoCs. Journal of Zhejiang University: Science A, 2008, 9, 1708-1714.	2.4	1
70	A partitioning approach to improve reconfigurable neuron-inspired online BIST. , 2010, , .		1
71	A Novel Modeling Approach for System-Level Application Mapping Targeted for Configurable Architecture. Canadian Journal of Electrical and Computer Engineering, 2014, 37, 192-202.	2.0	1
72	Early prediction of timing critical instructions in pipeline processor. , 2016, , .		1

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73	ESL, Back-annotating Crosstalk Fault Models into High-level Communication Links. , 2020, , .		1
74	Reconfiguration of Embedded Accelerators by Microprogramming for Intensive Loop Computations. , 2020, , .		1
75	n-DiCE-LSTM: An n-Dimensional Configurable and Efficient Architecture for LSTM Accelerator. , 2021, , .		1
76	Compiling gate RC models into a top level simulation model for rough timing analysis of VLSI circuits. Microprocessors and Microsystems, 1991, 15, 313-320.	2.8	0
77	ESTA: An Efficient Method for Reliability Enhancement of RT-Level Designs. Proceedings of the Asian Test Symposium, 2006, , .	0.0	0
78	Enhanced TED: A New Data Structure for RTL Verification. , 2008, , .		0
79	A Novel GA-Based High-Level Synthesis Technique to Enhance RT-Level Concurrent Testing. , 2008, , .		0
80	An advanced method for synthesizing TLM2-based interfaces. , 2008, , .		0
81	NoC Reconfiguration for Utilizing the Largest Fault-free Connected Sub-structure. , 2008, , .		0
82	Automating Hardware/Software partitioning using dependency Graph. , 2008, , .		0
83	A TLM2.0 assertion library with centralized monitoring approach. , 2010, , .		0
84	Using context based methods for test data compression. , 2010, , .		0
85	Adaptation of Standard RT Level BIST Architectures for System Level Communication Testing. , 2011, , .		0
86	Extracting complete set of equations to analyze VHDL-AMS descriptions. , 2013, , .		0
87	Application-specific power-aware mapping for reconfigurable NoC architectures. , 2015, , .		0
88	Universal mitigation of NBTI-induced aging by design randomization. , 2016, , .		0
89	Scalable Symbolic Simulation-Based Automatic Correction of Modern Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1845-1853.	3.1	0
90	Compensating Detection Latency of FPGA Scrubbers with a Collaborative Functional Hardware Duplication. , 2021, , .		0

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91	Integrating an Interconnect BIST with Crosstalk Avoidance Hardware. , 2021, , .		0
92	Reducing DFT hardware overhead by use of a test microprogram in a microprogrammed hardware accelerator. , 2020, , .		0
93	An HDL-Based Platform for High Level NoC Switch Testing. Proceedings of the Asian Test Symposium, 2007, , .	0.0	0
94	Concurrent Error Detection for LSTM Accelerators. , 2022, , .		0