Jcs Woo

List of Publications by Year
in descending order

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84 papers	1,784 citations	331259 21 h-index	301761 39 g-index
84 all docs	84 docs citations	84 times ranked	819 citing authors

#	Article	IF	Citations
1	Design of sub-100nm SOI CMOS for RF switch application. , 2013, , .		0
2	Characterization of copper germanide as contact metal for advanced MOSFETs. IEEE Electron Device Letters, 2006, 27, 549-551.	2.2	16
3	Dimensional scaling of nonlinear optical absorption in silicon waveguides. , 2005, , .		0
4	Effects of PAI on interface properties between HfSiO gate dielectric and silicon substrate. IEEE Transactions on Electron Devices, 2005, 52, 136-139.	1.6	2
5	A novel split-gate MOSFET design realized by a fully silicided gate process for the improvement of transconductance and output resistance. IEEE Electron Device Letters, 2005, 26, 829-831.	2.2	20
6	Source/drain resistance modeling in bulk and ultra-thin body SOI MOSFETs. , 2005, , .		1
7	Superior hot carrier reliability of single halo (SH) silicon-on-insulator (SOI) nMOSFET in analog applications. IEEE Transactions on Device and Materials Reliability, 2005, 5, 127-132.	1.5	16
8	Tunable work function in fully nickel-silicided polysilicon gates for metal gate MOSFET applications. IEEE Electron Device Letters, 2005, 26, 87-89.	2.2	19
9	A Device Design Methodology for Sub-100-nm SOC Applications Using Bulk and SOI MOSFETs. IEEE Transactions on Electron Devices, 2004, 51, 1122-1128.	1.6	17
10	TCAD-Based Statistical Analysis and Modeling of Gate Line-Edge Roughness Effect on Nanoscale MOS Transistor Performance and Scaling. IEEE Transactions on Semiconductor Manufacturing, 2004, 17, 192-200.	1.4	86
11	A/spl uml/nalysis of floating body effects in thin film conventional and single pocket SOI MOSFETs using the GIDL current technique. IEEE Electron Device Letters, 2002, 23, 209-211.	2.2	15
12	Source/Drain Parasitic Resistance Role and Electrical Coupling Effect in sub 50nm MOSFET Design. , 2002, , .		2
13	Optimization of Single Halo p-MOSFET Implant Parameters for Improved Analog Performance and Reliability. , 2002, , .		4
14	Detailed modeling of source/drain parasitics and their impact on MOSFETs scaling. , 2002, , .		0
15	Advanced model and analysis of series resistance for CMOS scaling into nanometer regime. I. Theoretical derivation. IEEE Transactions on Electron Devices, 2002, 49, 457-466.	1.6	66
16	Advanced model and analysis of series resistance for CMOS scaling into nanometer regime. II. Quantitative analysis. IEEE Transactions on Electron Devices, 2002, 49, 467-472.	1.6	72
17	Optimization and realization of sub-100-nm channel length single halo p-MOSFETs. IEEE Transactions on Electron Devices, 2002, 49, 1077-1079.	1.6	47
18	Channel engineering for analog device design in deep submicron CMOS technology for system on chip applications. IEEE Transactions on Electron Devices, 2002, 49, 1558-1565.	1.6	37

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19	Advanced source/drain engineering for box-shaped ultrashallow junction formation using laser annealing and pre-amorphization implantation in sub-100-nm SOI CMOS. IEEE Transactions on Electron Devices, 2002, 49, 1748-1754.	1.6	38
20	A study of hot-carrier induced interface-trap profiles in lateral asymmetric channel MOSFETs using a novel charge pumping technique. Solid-State Electronics, 2001, 45, 1717-1723.	0.8	12
21	Performance and hot-carrier reliability of 100 nm channel length jet vapor deposited Si/sub 3/N/sub 4/ MNSFETs. IEEE Transactions on Electron Devices, 2001, 48, 679-684.	1.6	12
22	Comprehensive study on low-frequency noise characteristics in surface channel SOI CMOSFETs and device design optimization for RF ICs. IEEE Transactions on Electron Devices, 2001, 48, 1428-1437.	1.6	38
23	The Effect of Impact Ionization on the Subthreshold Leakage Current in N-Channel Double-Gate SOI Transistors. , 2001, , .		0
24	Analog device design for low power mixed mode applications in deep submicron CMOS technology. IEEE Electron Device Letters, 2001, 22, 588-590.	2.2	27
25	Improvement of Flicker Noise in Lateral Asymmetric Channel N-MOSFETs for Sub-micron Analog Applications. , 2000, , .		2
26	AC floating body effects in partially depleted floating body SOI nMOS operated at elevated temperature: an analog circuit prospective. IEEE Electron Device Letters, 2000, 21, 494-496.	2.2	5
27	A study of 100 nm channel length asymmetric channel MOSFET by using charge pumping. Microelectronic Engineering, 1999, 48, 193-196.	1.1	11
28	Design considerations of high-Î² gate dielectrics for sub-0.1-Î¼m MOSFET's. IEEE Transactions on Electron Devices, 1999, 46, 261-262.	1.6	32
29	The impact of high-Î² gate dielectrics and metal gate electrodes on sub-100 nm MOSFETs. IEEE Transactions on Electron Devices, 1999, 46, 1537-1544.	1.6	271
30	AC floating body effects and the resultant analog circuit issues in submicron floating body and body-grounded SOI MOSFET's. IEEE Transactions on Electron Devices, 1999, 46, 1685-1692.	1.6	36
31	Floating body induced pre-kink excess low-frequency noise in submicron SOI CMOSFET technology. IEEE Electron Device Letters, 1999, 20, 484-486.	2.2	12
32	Exploration of velocity overshoot in a high-performance deep sub-0.1-Î¼m SOI MOSFET with asymmetric channel profile. IEEE Electron Device Letters, 1999, 20, 538-540.	2.2	35
33	Phase noise characteristics associated with low-frequency noise in submicron SOI MOSFET feedback oscillator for RF IC's. IEEE Electron Device Letters, 1999, 20, 54-56.	2.2	17
34	Advanced technologies for optimized sub-quarter-micrometer SOI CMOS devices. IEEE Transactions on Electron Devices, 1998, 45, 1092-1098.	1.6	7
35	A low thermal budget self-aligned Ti silicide technology using germanium implantation for thin-film SOI MOSFET's. IEEE Transactions on Electron Devices, 1998, 45, 1280-1286.	1.6	20
36	AC floating-body effects in submicron fully depleted (FD) SOI nMOSFETs and the impact on analog applications. IEEE Electron Device Letters, 1998, 19, 351-353.	2.2	15

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37	Empirical correlation between AC kink and low-frequency noise overshoot in SOI MOSFETs. IEEE Electron Device Letters, 1998, 19, 157-159.	2.2	16
38	An advanced Ge preamorphization salicide technology for ultra-thin-film SOI CMOS devices. IEEE Electron Device Letters, 1997, 18, 309-311.	2.2	11
39	Comparison of NMOS and PMOS hot carrier effects from 300 to 77 K. IEEE Transactions on Electron Devices, 1997, 44, 268-276.	1.6	71
40	Tunneling source-body contact for partially-depleted SOI MOSFET. IEEE Transactions on Electron Devices, 1997, 44, 1143-1147.	1.6	3
41	Hole confinement in a Si/GeSi/Si quantum well on SIMOX. IEEE Transactions on Electron Devices, 1996, 43, 180-182.	1.6	8
42	A novel salicide technology for thin film SOI MOSFETs using Ge pre-amorphization. , 1996, , .		3
43	Subthreshold characteristics of fully depleted submicrometer SOI MOSFET's. IEEE Transactions on Electron Devices, 1995, 42, 1120-1125.	1.6	36
44	Shallow buried channel gated BJT on TFSOI substrate. IEEE Electron Device Letters, 1994, 15, 391-393.	2.2	1
45	Modeling the I-V characteristics of fully depleted submicrometer SOI MOSFET's. IEEE Electron Device Letters, 1994, 15, 45-47.	2.2	34
46	High-mobility GeSi PMOS on SIMOX. IEEE Electron Device Letters, 1993, 14, 520-522.	2.2	48
47	High-gain lateral p-n-p bipolar action in a p-MOSFET structure. IEEE Electron Device Letters, 1992, 13, 312-313.	2.2	23
48	Enhancement-mode quantum-well Ge/sub x/Si/sub 1-x /PMOS. IEEE Electron Device Letters, 1991, 12, 154-156.	2.2	186
49	Optimization of LDD devices for cryogenic operation. IEEE Electron Device Letters, 1991, 12, 375-378.	2.2	6
50	Channel Mobility of Gesi Quantum-Well P-Mosfet's. , 1991, , .		2
51	Low frequency noise in quantum-well GexSi1â^'x PMOSFET's. Microelectronic Engineering, 1991, 15, 19-22.	1.1	6
52	High-gain lateral bipolar action in a MOSFET structure. IEEE Transactions on Electron Devices, 1991, 38, 2487-2496.	1.6	104
53	Bipolar transistors for low noise, low temperature electronics. Cryogenics, 1990, 30, 137-140.	0.9	5
54	Optimization of silicon bipolar transistors for high current gain at low temperatures. IEEE Transactions on Electron Devices, 1988, 35, 1311-1321.	1.6	50

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55	Short-channel effects in MOSFET's at liquid-Nitrogen temperature. IEEE Transactions on Electron Devices, 1986, 33, 1012-1019.	1.6	51
56	Dependence of LDD device optimization on stressing parameters at 77 K. , 0, , .		7
57	High-Mobility Gesi Quantum-Well Pmos on Simox. , 0, , .		1
58	A CMOS-compatible, low power and low noise gated BJT on TFSOI substrate. , 0, , .		0
59	A low thermal budget, fully self-aligned lateral BJT on thin film SOI substrate for low power BiCMOS applications. , 0, , .		4
60	Inversion hole mobility in fully depleted SOI PMOSFET's: measurement and modeling. , 0, , .		0
61	Parasitic bipolar turn-on of PD-SOI MOSFETs in dynamic logic circuits. , 0, , .		4
62	An alternative gate electrode material of fully depleted SOI CMOS for low power applications. , 0, , .		3
63	A general physical model for short-channel double-gate SOI MOSFETS. , 0, , .		0
64	The impact of SOI MOSFETs on low power digital circuits. , 0, , .		1
65	Comprehensive study on AC characteristics in SOI MOSFETs for analog applications. , 0, , .		10
66	Sub-0.18 Î¼m SOI MOSFETs using lateral asymmetric channel profile and Ge pre-amorphization salicide technology. , 0, , .		9
67	Device design methodology to optimize low-frequency noise in advanced SOI CMOS technology for RF ICs. , 0, , .		4
68	60 nm Î“-gate MOSFETs with self-aligned drain extension formed by solid phase diffusion. , 0, , .		0
69	Channel engineering for high speed sub-1.0 V power supply deep sub-micron CMOS. , 0, , .		20
70	Minimizing body instability in deep sub-micron SOI MOSFETs for sub-1 V RF applications. , 0, , .		4
71	Temperature dependence of AC floating body effects in PD SOI nMOS. , 0, , .		2
72	100 nm channel length MNSFETs using a jet vapor deposited ultra-thin silicon nitride gate dielectric. , 0, , .		10

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73	Advanced silicide for sub-0.18 Î¼m CMOS on ultra-thin (35 Î¼m) SOI. , 0, , .		0
74	Advanced model and analysis for series resistance in sub-100 nm CMOS including poly depletion and overlap doping gradient effect. , 0, , .		9
75	Sub-micron fully depleted lateral asymmetric channel SOI MOSFETs for analog and mixed mode applications. , 0, , .		2
76	Reliability studies on sub 100 nm SOI-MNSFETs. , 0, , .		0
77	Novel sub-25 nm devices [MOSFETs]. , 0, , .		0
78	50 nm SOI CMOS transistors with ultra shallow junction using laser annealing and pre-amorphization implantation. , 0, , .		7
79	Enhanced subthreshold leakage current due to impact ionization in deep sub-100nm N-channel double-gate MOSFETs. , 0, , .		1
80	Novel direct-tunneling-current (DTC) method for channel length extraction beyond sub-50nm gate CMOS. , 0, , .		1
81	Scaling impact on analog performance of sub-100nm MOSFETs for mixed mode applications. , 0, , .		8
82	Comparison between bulk and SOI MOSFETs for sub-100nm mixed mode applications. , 0, , .		0
83	Analog performance of scaled bulk and SOI MOSFETs. , 0, , .		3
84	Novel Device structures for Sub-25nm Generation. , 0, , .		0