M Balakrishnan

List of Publications by Year
in descending order

66 papers	540 citations	1040056 9 h-index	940533 16 g-index
66 all docs	66 docs citations	66 times ranked	369 citing authors

#	Article	IF	Citations
1	Standardizing the approach to late onset sepsis in neonates through antimicrobial stewardship: a quality improvement initiative. Journal of Perinatology, 2020, 40, 1433-1440.	2.0	11
2	ML Guided Energy-Performance Trade-Off Estimation For Uncore Frequency Scaling. , 2019, , .		4
3	Evaluating the Use of Variable Height in Tactile Graphics. , 2019, , .		3
4	Majority Logic: Prime Implicants and n-Input Majority Term Equivalence. , 2019, , .		3
5	GRanDE: Graphical Representation and Design Space Exploration of Embedded Systems. , 2019, , .		0
6	Equivalence Checking and Compaction of n-input Majority Terms Using Implicants of Majority. Journal of Electronic Testing: Theory and Applications (JETTA), 2019, 35, 679-694.	1.2	0
7	Tactile Diagrams for the Visually Impaired. IEEE Potentials, 2017, 36, 14-18.	0.3	18
8	Promoting teamwork may improve infant care processes during delivery room management: Florida perinatal quality collaborativeâ€™s approach. Journal of Perinatology, 2017, 37, 886-892.	2.0	16
9	Optimal mapping of program overlays onto many-core platforms with limited memory capacity. Design Automation for Embedded Systems, 2017, 21, 173-194.	1.0	1
10	Leakage Power Aware Task Assignment Algorithms for Multicore Platforms. , 2016, , .		4
11	Configurable Architectures for Multi-Mode Floating Point Adders. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2079-2090.	5.4	6
12	High Level Design Approach to Accelerate De Novo Genome Assembly Using FPGAs. , 2014, , .		1
13	Configurable Architecture for Double/Two-Parallel Single Precision Floating Point Division. , 2014, , .		6
14	Mapping Tasks to a Dynamically Reconfigurable Coarse Grained Array. , 2014, , .		2
15	LightSim: A leakage aware ultrafast temperature simulator. , 2014, , .		16
16	Unified Architecture for Double/Two-Parallel Single Precision Floating Point Adder. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 521-525.	3.0	16
17	Accelerating Genome Assembly Using Hard Embedded Blocks in FPGAs. , 2014, , .		7
18	Series Expansion based Efficient Architectures for Double Precision Floating Point Division. Circuits, Systems, and Signal Processing, 2014, 33, 3499-3526.	2.0	7

#	Article	IF	Citations
19	Accelerating 3D-FFT Using Hard Embedded Blocks in FPGAs. , 2013, , .		8
20	FAssem: FPGA Based Acceleration of De Novo Genome Assembly. , 2013, , .		20
21	Design and Implementation of High Performance Architectures with Partially Reconfigurable CGRAs. , 2013, , .		2
22	Performance Estimation of GPUs with Cache. , 2012, , .		15
23	System-Level Design Space Exploration Methodology for Energy-Efficient Sensor Node Configurations: An Experimental Validation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 586-596.	2.7	4
24	Compressing Cache State for Postsilicon Processor Debug. IEEE Transactions on Computers, 2011, 60, 484-497.	3.4	3
25	Blood urea nitrogen and serum bicarbonate in extremely low birth weight infants receiving higher protein intake in the first week after birth. Journal of Perinatology, 2011, 31, 535-539.	2.0	23
26	A tiled programmable fabric using QCA. , 2010, , .		0
27	Enhancing post-silicon processor debug with Incremental Cache state Dumping. , 2010, , .		2
28	A generic platform for estimation of multi-threaded program performance on heterogeneous multiprocessors. , 2009, , .		4
29	FPGA accelerator for protein structure prediction algorithm. , 2009, , .		11
30	Integrated energy analysis of error correcting codes and modulation for energy efficient wireless sensor nodes. IEEE Transactions on Wireless Communications, 2009, 8, 5348-5355.	9.2	47
31	Cache aware compression for processor debug support. , 2009, , .		6
32	A Framework for Energy-Consumption-Based Design Space Exploration for Wireless Sensor Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1017-1024.	2.7	52
33	Evaluation of Bus Based Interconnect Mechanisms in Clustered VLIW Architectures. International Journal of Parallel Programming, 2007, 35, 507-527.	1.5	1
34	An Efficient Technique for Exploring Register File Size in ASIP Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 1693-1699.	2.7	3
35	Exploring storage organization in ASIP synthesis. , 2003, , .		3
36	Analysis of the influence of register file size on energy consumption, code size, and execution time. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2001, 20, 1329-1337.	2.7	26

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37	A STUDY OF EFFICACY OF HETEROGENEOUS BONE GRAFTS (SURGIBONE) IN ORTHOPAEDIC SURGERY. Medical Journal Armed Forces India, 2000, 56, 21-23.	0.8	3
38	Simulation and modeling of a multicast ATM switch. , 1999, , .		0
39	SALMONELLA SENFTENBERG OSTEOMYELITIS. Medical Journal Armed Forces India, 1999, 55, 153-154.	0.8	0
40	OSTEOID OSTEOMA IN NECK OF FEMUR. Medical Journal Armed Forces India, 1999, 55, 163-164.	0.8	2
41	EXTERNAL FIXATION OF INTERTROCHANTERIC FRACTURES OF FEMUR IN ELDERLY. Medical Journal Armed Forces India, 1999, 55, 325-327.	0.8	1
42	AN UNUSUAL CASE OF FRACTURE DISLOCATION NECK OF TALUS. Medical Journal Armed Forces India, 1999, 55, 270-272.	0.8	0
43	Direct mapping of RTL structures onto LUT-based FPGA's. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1998, 17, 624-631.	2.7	15
44	An efficient retargetable microprogram generating system. Microprocessing and Microprogramming, 1987, 19, 305-318.	0.2	2
45	A survey of microprogramming languages. Microprocessing and Microprogramming, 1986, 17, 19-27.	0.2	2
46	An efficient retargetable microcode generator. ACM SIGMICRO Newsletter, 1986, 17, 44-53.	0.4	1
47	DESSERT: Design Space Exploration of RT Level Components. , 0, , .		4
48	Optimal clock period for synthesized data paths. , 0, , .		5
49	A novel reconfigurable co-processor architecture. , 0, , .		4
50	Allocation of FIFO structures in RTL data paths. , 0, , .		3
51	Real time collision detection and avoidance. A case study for design space exploration in HW-SW codesign. , 0, , .		0
52	Optimal hardware/software partitioning for concurrent specification using dynamic programming. , 0, , .		6
53	Interface synthesis: issues and approaches. , 0, , .		15
54	Processor evaluation in an embedded systems design environment. , 0, , .		27

#	Article	IF	Citations
55	ASIP design methodologies: survey and issues. , 0, , .		71
56	A specialized graduate program in VLSI design: a success story. , 0, , .		0
57	Integrating communication cost estimation in embedded systems design: a PCI case study. , 0, , .		0
58	Evaluating register file size in ASIP design. , 0, , .		3
59	Exploring the number of register windows in ASIP synthesis. , 0, , .		3
60	A new divide and conquer method for achieving high speed division in hardware. , 0, , .		0
61	SoC synthesis with automatic hardware-software interface generation. , 0, , .		5
62	Synthesis of application specific multiprocessor architectures for process networks. , 0, , .		1
63	Evaluation of Bus Based Interconnect Mechanisms in Clustered VLIW Architectures. , 0, , .		8
64	A Specialized Graduate Program in VLSI Design Tools and Technology. , 0, , .		0
65	Integrated on-chip storage evaluation in ASIP synthesis. , 0, , .		5
66	Rapid Resource-Constrained Hardware Performance Estimation. , 0, , .		3