Wonyong Sung

List of Publications by Citations

88 papers	1,265 citations	18 h-index	33 g-index
134 ext. papers	1,604 ext. citations	2.6 avg, IF	4.88 L-index

#	Paper	IF	Citations
88	Simulation-based word-length optimization method for fixed-point digital signal processing systems. *IEEE Transactions on Signal Processing*, **1995**, 43, 3087-3090	4.8	111
87	Fixed-point feedforward deep neural network design using weights +1, 0, and 1 **2014**,		106
86	Fixed point optimization of deep convolutional neural networks for object recognition **2015**,		85
85	Combined word-length optimization and high-level synthesis of digital signal processing systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2001**, 20, 921-930	2.5	83
84	Low-Power High-Throughput BCH Error Correction VLSI Design for Multi-Level Cell NAND Flash Memories **2006**,		82
83	Estimation of NAND Flash Memory Threshold Voltage Distribution for Optimum Soft-Decision Error Correction. *IEEE Transactions on Signal Processing*, **2013**, 61, 440-449	4.8	61
82	VLSI Implementation of BCH Error Correction for Multilevel Cell NAND Flash Memory. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 843-847	2.6	58
81	Memory Access Optimized Implementation of Cyclic and Quasi-Cyclic LDPC Codes on a GPGPU. *Journal of Signal Processing Systems*, **2011**, 64, 149-159	1.4	48
80	FPGA-Based Low-Power Speech Recognition with Recurrent Neural Networks **2016**,		44
79	AUTOSCALER for C: an optimizing floating-point to integer C program converter for fixed-point digital signal processors. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2000**, 47, 840-848		40
78	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 1004-1015	2.6	38
77	FPGA based implementation of deep neural networks using on-chip memory only **2016**,		35
76	Efficient Software-Based Encoding and Decoding of BCH Codes. *IEEE Transactions on Computers*, **2009**, 58, 878-889	2.5	22
75	Dynamic hand gesture recognition for wearable devices with low complexity recurrent neural networks **2016**,		20
74	A high-speed layered min-sum LDPC decoder for error correction of NAND Flash memories **2011**,		20
73	A Real-Time FPGA-Based 20 000-Word Speech Recognizer With Optimized DRAM Access. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2010**, 57, 2119-2131	3.9	20
72	Single stream parallelization of generalized LSTM-like RNNs on a GPU **2015**,		19

71	Adaptive Threshold Technique for Bit-Flipping Decoding of Low-Density Parity-Check Codes. *IEEE Communications Letters*, **2010**, 14, 857-859	3.8	18
70	Decision Directed Estimation of Threshold Voltage Distribution in NAND Flash Memory. *IEEE Transactions on Signal Processing*, **2014**, 62, 919-927	4.8	17
69	Performance of rate 0.96 (68254, 65536) EG-LDPC code for NAND Flash memory error correction **2012**,		17
68	X1000 real-time phoneme recognition VLSI using feed-forward deep neural networks **2014**,		16
67	Load Balanced Resampling for Real-Time Particle Filtering on Graphics Processing Units. *IEEE Transactions on Signal Processing*, **2013**, 61, 411-419	4.8	16
66	. *IEEE Transactions on Circuits and Systems for Video Technology*, **1998**, 8, 935-940	6.4	14
65	Character-level incremental speech recognition with recurrent neural networks **2016**,		13
64	A voice activity detector employing soft decision based noise spectrum adaptation		13
63	Character-level language modeling with hierarchical recurrent neural networks **2017**,		12
62	An FPGA implementation of speech recognition with weighted finite state transducers **2010**,		12
61	Fault tolerance analysis of digital feed-forward deep neural networks **2014**,		11
60	Memory access pattern-aware DRAM performance model for multi-core systems **2011**,		11
59	VLSI for 5000-word continuous speech recognition **2009**,		11
58	Fixed-point optimization of deep neural networks with adaptive step size retraining **2017**,		10
57	Least Squares Based Coupling Cancelation for MLC NAND Flash Memory with a Small Number of Voltage Sensing Operations. *Journal of Signal Processing Systems*, **2013**, 71, 189-200	1.4	9
56	Fixed-point optimization utility for C and C++ based digital signal processing programs		9
55	VLSI Implementation of a High-Throughput Soft-Bit-Flipping Decoder for Geometric LDPC Codes. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2010**, 57, 1083-1094	3.9	8
54	Least squares based cell-to-cell interference cancelation technique for multi-level cell nand flash memory **2012**,		8

53	Massively parallel implementation of cyclic LDPC codes on a general purpose graphics processing unit **2009**,		8
52	OpenMP-based parallel implementation of a continuous speech recognizer on a multi-core system **2009**,		8
51	Structured sparse ternary weight coding of deep neural networks for efficient hardware implementations **2017**,		7
50	Memory Access Optimized VLSI for 5000-Word Continuous Speech Recognition. *Journal of Signal Processing Systems*, **2011**, 63, 95-105	1.4	6
49	Error performance and decoder hardware comparison between EG-LDPC and BCH codes **2010**,		6
48	Fixed-Point Optimization of Transformer Neural Network **2020**,		5
47	H- and C-level WFST-based large vocabulary continuous speech recognition on Graphics Processing Units **2011**,		5
46	Low-power implementation of a high-throughput LDPC decoder for IEEE 802.11N standard **2009**,		5
45	Performance Evaluation of an SIMD Architecture with a Multi-bank Vector Memory Unit. *Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on*, **2006**,		5
44	A CORDIC-based digital quadrature mixer: comparison with a ROM-based architecture		5
43	Flexible and Expandable Speech Recognition Hardware with Weighted Finite State Transducers. *Journal of Signal Processing Systems*, **2012**, 66, 235-244	1.4	4
42	Block-interleaving based parallel CRC computation for multi-processor systems **2010**,		4
41	Fixed-point C compiler for TMS320C50 digital signal processor		4
40	VLSI design of a CORDIC-based derotator		4
39	Memorization Capacity of Deep Neural Networks under Parameter Quantization **2019**,		3
38	Soft-decision decoding with cell to cell interference removed signal in nand flash memory **2013**,		3
37	Reduced complexity Chase-Pyndiah decoding algorithm for turbo product codes **2011**,		3
36	SIMD processor based implementation of recursive filtering equations **2009**,		3

35	Scalable HMM based inference engine in large vocabulary continuous speech recognition **2009**,		3
34	Access-Pattern-Aware On-Chip Memory Allocation for SIMD Processors. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2009**, 28, 158-163	2.5	3
33	Optimized timed hardware software cosimulation without roll-back		3
32	Architectural Design and Implementation of an FPGA Softcore Based Speech Recognition System **2006**,		3
31	H.264 decoder optimization exploiting SIMD instructions		3
30	Software optimization of MPEG audio layer-III for a 32 bit RISC processor		3
29	Soft-Decision Error Correction of NAND Flash Memory with a Turbo Product Code. *Journal of Signal Processing Systems*, **2013**, 70, 235-247	1.4	2
28	Multi-user real-time speech recognition with a GPU **2012**,		2
27	COPR: a cost-oriented recycling policy for flash translation layer. *IEEE Transactions on Consumer Electronics*, **2010**, 56, 673-681	4.8	2
26	Algorithm and Software Optimization of Variable Block Size Motion Estimation for H.264/AVC on a VLIW SIMD DSP. *Journal of Signal Processing Systems*, **2008**, 51, 289-302	1.4	2
25	Mobile CPU Based Optimization of Fast Likelihood Computation for Continuous Speech Recognition **2007**,		2
24	VLSI Implementation of An Adaptive Equalizer for ATSC Digital TV Receivers. *Journal of Signal Processing Systems*, **2005**, 40, 301-310		2
23	A Compiler-Friendly RISC-Based Digital Signal Processor Synthesis and Performance Evaluation. *Journal of Signal Processing Systems*, **2001**, 27, 297-312		2
22	A floating-point to integer C converter with shift reduction for fixed-point digital signal processors **1999**,		2
21	Optimum wordlength determination of 8/spl times/8 IDCT architectures conforming to the IEEE standard specifications		2
20	Learning separable fixed-point kernels for deep convolutional neural networks **2016**,		1
19	Workload-aware Automatic Parallelization for Multi-GPU DNN Training **2019**,		1
18	Signal processing techniques for reliability improvement of sub-20NM NAND flash memory **2013**,		1

17	High-throughput decoding of block turbo codes on graphics processing units **2017**,		1
16	Direct and indirect measurement of inter-cell capacitance in NAND flash memory **2014**,		1
15	Parallel Computation of Adaptive Filtering Algorithms on Multi-Core Systems. *Journal of Signal Processing Systems*, **2012**, 69, 253-265	1.4	1
14	GPU based implementation of recursive digital filtering algorithms **2013**,		1
13	Multi-core and SIMD architecture based implementation of recursive digital filtering algorithms **2010**,		1
12	VLSI implementation of a soft bit-flipping decoder for PG-LDPC codes **2009**,		1
11	A hardware software cosimulation backplane with automatic interface generation		1
10	An efficient compiled simulation system for VLIW code verification		1
9	Fast Block Mode Decision for H.264/AVC on a Programmable Digital Signal Processor. *Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on*, **2007**,		1
8	Memory access overhead reduction for a digital color copier implementation using a VLIW digital signal processor		1
7	Finite wordlength effects analysis and wordlength optimization of a multiplier-adder based 8/spl times/8 2D-IDCT architecture		1
6	Low Energy Signal Processing Techniques for Reliability Improvement of High-Density NAND Flash Memory. *Journal of Signal Processing Systems*, **2015**, 78, 63-71	1.4	
5	Area-Efficient Parallel Syndrome Generators for Linear Block Codes. *Journal of Signal Processing Systems*, **2014**, 77, 281-287	1.4	
4	Optimization of Number Representations **2019**, 1141-1171		
3	Optimization of Number Representations **2010**, 707-738		
2	Optimization of Number Representations **2013**, 1303-1333		
1	Compression of Deep Neural Networks with Structured Sparse Ternary Coding. *Journal of Signal Processing Systems*, **2019**, 91, 1009-1019	1.4	