Tsu-Jae King Liu

List of Publications by Citations

143 papers	4,078 citations	30 h-index	60 g-index
153 ext. papers	4,931 ext. citations	3.3 avg, IF	5.38 L-index

#	Paper	IF	Citations
143	Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec. *IEEE Electron Device Letters*, **2007**, 28, 743-745	4.4	1160
142	. *Proceedings of the IEEE*, **2008**, 96, 306-322	14.3	173
141	. *IEEE Journal of Solid-State Circuits*, **2011**, 46, 308-320	5.5	145
140	Tunnel Field Effect Transistor With Raised Germanium Source. *IEEE Electron Device Letters*, **2010**, 31, 1107-1109	4.4	113
139	. *IEEE Transactions on Electron Devices*, **2011**, 58, 3541-3548	2.9	110
138	. *Proceedings of the IEEE*, **2010**, 98, 2076-2094	14.3	96
137	Large-Scale SRAM Variability Characterization in 45 nm CMOS. *IEEE Journal of Solid-State Circuits*, **2009**, 44, 3174-3192	5.5	94
136	Study of Random Dopant Fluctuation Induced Variability in the Raised-Ge-Source TFET. *IEEE Electron Device Letters*, **2013**, 34, 184-186	4.4	92
135	Integrated circuit design with NEM relays **2008**,		83
134	. *IEEE Transactions on Electron Devices*, **2011**, 58, 236-250	2.9	76
133	**2009**,		71
132	Gate Line Edge Roughness Model for Estimation of FinFET Performance Variability. *IEEE Transactions on Electron Devices*, **2009**, 56, 3055-3063	2.9	70
131	Study of Random-Dopant-Fluctuation (RDF) Effects for the Trigate Bulk MOSFET. *IEEE Transactions on Electron Devices*, **2009**, 56, 1538-1542	2.9	66
130	Design and reliability of a micro-relay technology for zero-standby-power digital logic applications **2009**,		61
129	Nanoelectromechanical Switches for Low-Power Digital Computing. *Micromachines*, **2015**, 6, 1046-1065	3.3	54
128	A Comparative Study of Dopant-Segregated Schottky and Raised Source/Drain Double-Gate MOSFETs. *IEEE Transactions on Electron Devices*, **2008**, 55, 2665-2677	2.9	50
127	Prospect of tunneling green transistor for 0.1V CMOS **2010**,		47

126	. *IEEE Transactions on Electron Devices*, **2011**, 58, 3294-3299	2.9	45
125	Tri-Gate Bulk MOSFET Design for CMOS Scaling to the End of the Roadmap. *IEEE Electron Device Letters*, **2008**, 29, 491-493	4.4	45
124	Characterization of Dynamic SRAM Stability in 45 nm CMOS. *IEEE Journal of Solid-State Circuits*, **2011**, 46, 2702-2712	5.5	42
123	Nano-Electro-Mechanical Nonvolatile Memory (NEMory) Cell Design and Scaling. *IEEE Transactions on Electron Devices*, **2008**, 55, 3482-3488	2.9	41
122	A new switching device for printed electronics: inkjet-printed microelectromechanical relay. *Nano Letters*, **2013**, 13, 5355-60	11.5	38
121	Mechanically modulated tunneling resistance in monolayer MoS2. *Applied Physics Letters*, **2013**, 103, 183105	3.4	36
120	Perfectly Complementary Relay Design for Digital Logic Applications. *IEEE Electron Device Letters*, **2010**, 31, 371-373	4.4	36
119	Characterization of Contact Resistance Stability in MEM Relays With Tungsten Electrodes. *Journal of Microelectromechanical Systems*, **2012**, 21, 511-513	2.5	36
118	Dopant-Segregated Schottky Source/Drain Double-Gate MOSFET Design in the Direct Source-to-Drain Tunneling Regime. *IEEE Transactions on Electron Devices*, **2009**, 56, 2016-2026	2.9	34
117	Effectiveness of Stressors in Aggressively Scaled FinFETs. *IEEE Transactions on Electron Devices*, **2012**, 59, 1592-1598	2.9	33
116	Demonstration of integrated micro-electro-mechanical switch circuits for VLSI applications **2010**,		33
115	FinFET Evolution Toward Stacked-Nanowire FET for CMOS Technology Scaling. *IEEE Transactions on Electron Devices*, **2015**, 62, 3945-3950	2.9	31
114	Performance and Area Scaling Benefits of FD-SOI Technology for 6-T SRAM Cells at the 22-nm Node. *IEEE Transactions on Electron Devices*, **2010**, 57, 1301-1309	2.9	30
113	Compact Nano-Electro-Mechanical Non-Volatile Memory (NEMory) for 3D Integration **2007**,		29
112	Design Optimization of Multigate Bulk MOSFETs. *IEEE Transactions on Electron Devices*, **2013**, 60, 28-33	2.9	27
111	Adhesive Force Characterization for MEM Logic Relays With Sub-Micron Contacting Regions. *Journal of Microelectromechanical Systems*, **2014**, 23, 198-203	2.5	27
110	Hybrid CMOS/BEOL-NEMS technology for ultra-low-power IC applications **2014**,		26
109	The relay reborn. *IEEE Spectrum*, **2012**, 49, 40-43	1.7	25

108	Seesaw Relay Logic and Memory Circuits. *Journal of Microelectromechanical Systems*, **2010**, 19, 1012-1014	2.5	25
107	Impact of Body Doping and Thickness on the Performance of Germanium-Source TFETs. *IEEE Transactions on Electron Devices*, **2010**, 57, 1710-1713	2.9	25
106	ZrO2 Ferroelectric FET for Non-volatile Memory Application. *IEEE Electron Device Letters*, **2019**, 40, 1419-1422	4.4	24
105	Comparison of SOI Versus Bulk FinFET Technologies for 6T-SRAM Voltage Scaling at the 7-/8-nm Node. *IEEE Transactions on Electron Devices*, **2017**, 64, 329-332	2.9	23
104	Characterization of Polycrystalline Silicon-Germanium Film Deposition for Modularly Integrated MEMS Applications. *Journal of Microelectromechanical Systems*, **2007**, 16, 68-77	2.5	21
103	Analysis of 7/8-nm Bulk-Si FinFET Technologies for 6T-SRAM Scaling. *IEEE Transactions on Electron Devices*, **2016**, 63, 1502-1507	2.9	21
102	. *IEEE Transactions on Electron Devices*, **2017**, 64, 1323-1329	2.9	19
101	. *IEEE Transactions on Electron Devices*, **2011**, 58, 1846-1854	2.9	19
100	Four-Terminal-Relay Body-Biasing Schemes for Complementary Logic Circuits. *IEEE Electron Device Letters*, **2010**, 31, 890-892	4.4	18
99	Sub-50 mV NEM relay operation enabled by self-assembled molecular coating **2016**,		18
98	Carrier-Mobility Enhancement via Strain Engineering in Future Thin-Body MOSFETs. *IEEE Electron Device Letters*, **2012**, 33, 318-320	4.4	17
97	Design Requirements for Steeply Switching Logic Devices. *IEEE Transactions on Electron Devices*, **2012**, 59, 326-334	2.9	17
96	Spacer Gate Lithography for Reduced Variability Due to Line Edge Roughness. *IEEE Transactions on Semiconductor Manufacturing*, **2010**, 23, 311-315	2.6	17
95	Scaling Limitations for Flexural Beams Used in Electromechanical Devices. *IEEE Transactions on Electron Devices*, **2009**, 56, 688-691	2.9	16
94	Three-Dimensional FinFET Source/Drain and Contact Design Optimization Study. *IEEE Transactions on Electron Devices*, **2009**, 56, 1483-1492	2.9	16
93	Analysis and demonstration of MEM-relay power gating **2010**,		15
92	Dopant-Segregated Schottky Junction Tuning With Fluorine Pre-Silicidation Ion Implant. *IEEE Transactions on Electron Devices*, **2010**, 57, 1084-1092	2.9	15
91	Nanocrystal-Embedded-Insulator (NEI) Ferroelectric Field-Effect Transistor Featuring Low Operating Voltages and Improved Synaptic Behavior. *IEEE Electron Device Letters*, **2019**, 40, 1933-1936	4.4	14

90	Planar GeOI TFET Performance Improvement With Back Biasing. *IEEE Transactions on Electron Devices*, **2012**, 59, 1629-1635	2.9	14
89	Comparative Study of Uniform Versus Supersteep Retrograde MOSFET Channel Doping and Implications for 6-T SRAM Yield. *IEEE Transactions on Electron Devices*, **2013**, 60, 1790-1793	2.9	14
88	Simulation-Based Study of the Inserted-Oxide FinFET for Future Low-Power System-on-Chip Applications. *IEEE Electron Device Letters*, **2015**, 36, 742-744	4.4	14
87	Nanomechanical Switch Designs to Overcome the Surface Adhesion Energy Limit. *IEEE Electron Device Letters*, **2015**, 36, 963-965	4.4	14
86	Four-Terminal Relay Design for Improved Body Effect. *IEEE Electron Device Letters*, **2010**, 31, 515-517	4.4	14
85	Non-Volatile Nano-Electro-Mechanical Memory for Energy-Efficient Data Searching. *IEEE Electron Device Letters*, **2016**, 37, 31-34	4.4	13
84	Effect of Body Biasing on the Energy-Delay Performance of Logic Relays. *IEEE Electron Device Letters*, **2015**, 36, 862-864	4.4	13
83	Variation-Aware Comparative Study of 10-nm GAA Versus FinFET 6-T SRAM Performance and Yield. *IEEE Transactions on Electron Devices*, **2014**, 61, 3949-3954	2.9	13
82	Highly scaled (Lg~56nm) gate-last Si tunnel field-effect transistors with ION>100Â/Îm. *Solid-State Electronics*, **2011**, 65-66, 22-27	1.7	13
81	High-Mobility Ge pMOSFETs With Crystalline ZrO2 Dielectric. *IEEE Electron Device Letters*, **2019**, 40, 371-374	4.4	12
80	Design of Gate-All-Around Silicon MOSFETs for 6-T SRAM Area Efficiency and Yield. *IEEE Transactions on Electron Devices*, **2014**, 61, 2371-2377	2.9	12
79	Electromechanical Diode Cell for Cross-Point Nonvolatile Memory Arrays. *IEEE Electron Device Letters*, **2012**, 33, 131-133	4.4	12
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77	. *IEEE Transactions on Electron Devices*, **2011**, 58, 3283-3285	2.9	12
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75	Back-End-of-Line Nano-Electro-Mechanical Switches for Reconfigurable Interconnects. *IEEE Electron Device Letters*, **2020**, 41, 625-628	4.4	11
74	Physically Based Modeling of Stress-Induced Variation in Nanoscale Transistor Performance. *IEEE Transactions on Device and Materials Reliability*, **2011**, 11, 378-386	1.6	11
73	Channel Stress and Ballistic Performance Advantages of Gate-All-Around FETs and Inserted-Oxide FinFETs. *IEEE Nanotechnology Magazine*, **2017**, 16, 209-216	2.6	10

72	Impact of Gate Line-Edge Roughness (LER) Versus Random Dopant Fluctuations (RDF) on Germanium-Source Tunnel FET Performance. *IEEE Nanotechnology Magazine*, **2013**, 12, 1061-1067	2.6	10
71	Multi-input/multi-output relay design for more compact and versatile implementation of digital logic with zero leakage **2012**,		10
70	Stable ruthenium-contact relay technology for low-power logic **2013**,		10
69	The Effect of Random Dopant Fluctuation on Specific Contact Resistivity. *IEEE Transactions on Electron Devices*, **2010**, 57, 273-281	2.9	10
68	Study of bending-induced strain effects on MuGFET performance. *IEEE Electron Device Letters*, **2006** , 27, 671-673	4.4	10
67	Nanocrystal-Embedded-Insulator Ferroelectric Negative Capacitance FETs With Sub-kT/q Swing. *IEEE Electron Device Letters*, **2018**, 1-1	4.4	10
66	Embedded Nano-Electro-Mechanical Memory for Energy-Efficient Reconfigurable Logic. *IEEE Electron Device Letters*, **2016**, 37, 1563-1565	4.4	9
65	Extension of Planar Bulk n-Channel MOSFET Scaling With Oxygen Insertion Technology. *IEEE Transactions on Electron Devices*, **2014**, 61, 3345-3349	2.9	9
64	Interfacial Adhesion between Rough Surfaces of Polycrystalline Silicon and Its Implications for M/NEMS Technology. *Journal of Adhesion Science and Technology*, **2010**, 24, 2545-2556	2	9
63	Scale-Length Assessment of the Trigate Bulk MOSFET Design. *IEEE Transactions on Electron Devices*, **2009**, 56, 2840-2842	2.9	9
62	Impact of Gate-Induced Strain on MuGFET Reliability. *IEEE Electron Device Letters*, **2008**, 29, 916-919	4.4	9
61	Selective Enhancement of SiO[sub 2] Etch Rate by Ar-Ion Implantation for Improved Etch Depth Control. *Electrochemical and Solid-State Letters*, **2007**, 10, D89		9
60	Prospects for MEM logic switch technology **2010**,		8
59	DSS MOSFET With Tunable SDE Regions by Fluorine Pre-Silicidation Ion Implant. *IEEE Electron Device Letters*, **2010**, 31, 785-787	4.4	8
58	Enhanced endurance of dual-bit SONOS NVM cells using the GIDL read method **2008**,		8
57	Energy-delay performance optimization of NEM logic relay **2015**,		7
56	Reliability of MEM relays for zero leakage logic **2013**,		7
55	Quasi-planar bulk CMOS technology for improved SRAM scalability. *Solid-State Electronics*, **2011**, 65-66, 184-190	1.7	7

54	There's plenty of room at the top **2017**,		6
53	Variability Study for Low-Voltage Microelectromechanical Relay Operation. *IEEE Transactions on Electron Devices*, **2018**, 65, 1529-1534	2.9	6
52	Microelectromechanical Relay and Logic Circuit Design for Zero Crowbar Current. *IEEE Transactions on Electron Devices*, **2014**, 61, 3296-3302	2.9	6
51	NEM relay design for compact, ultra-low-power digital logic circuits **2014**,		6
50	MOSFET performance and scalability enhancement by insertion of oxygen layers **2012**,		6
49	**2011**,		6
48	Reliability of Nanoelectromechanical Nonvolatile Memory (NEMory) Cells. *IEEE Electron Device Letters*, **2009**, 30, 269-271	4.4	6
47	FinFET Design for Tolerance to Statistical Dopant Fluctuations. *IEEE Nanotechnology Magazine*, **2009**, 8, 375-378	2.6	6
46	FinFET Performance Enhancement with Tensile Metal Gates and Strained Silicon on Insulator (sSOI) Substrate **2006**,		6
45	Threshold Voltage and DIBL Variability Modeling Based on Forward and Reverse Measurements for SRAM and Analog MOSFETs. *IEEE Transactions on Electron Devices*, **2015**, 62, 1119-1126	2.9	5
44	Tilted ion implantation as a cost-efficient sublithographic patterning technique. *Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics*, **2016**, 34, 040608	1.3	5
43	. *IEEE Transactions on Electron Devices*, **2012**, 59, 1468-1474	2.9	5
42	Examining the Self-Efficacy of Community College STEM Majors: Factors Related to Four-Year Degree Attainment. *Community College Journal of Research and Practice*, **2015**, 39, 1111-1124	0.6	5
41	Electron mobility enhancement in (100) oxygen-inserted silicon channel. *Applied Physics Letters*, **2015**, 107, 123502	3.4	5
40	Extending CMOS with negative capacitance56-76		5
39	Recent progress and challenges for relay logic switch technology **2012**,		5
38	Fabrication of $hbox{Si}_{1 - x}hbox{Ge}_{x}/hbox{Si}$ pMOSFETs Using Corrugated Substrates for Improved $I_{rm ON}$ and Reduced Layout-Width Dependence. *IEEE Transactions on Electron Devices*, **2013**, 60, 153-158	2.9	5
37	Sub-60nm Si tunnel field effect transistors with Ion >100 μA/μm **2010**,		5

36	Tri-gate bulk CMOS technology for improved SRAM scalability **2010**,		5
35	Dual-Bit Gate-Sidewall Storage FinFET NVM and New Method of Charge Detection. *IEEE Electron Device Letters*, **2007**, 28, 502-505	4.4	5
34	Reducing adhesion energy of nano-electro-mechanical relay contacts by self-assembled Perfluoro (2,3-Dimethylbutan-2-ol) coating. *AIP Advances*, **2019**, 9, 055329	1.5	4
33	Electromechanical Diode Cell Scaling for High-Density Nonvolatile Memory. *IEEE Transactions on Electron Devices*, **2014**, 61, 1382-1387	2.9	4
32	First Demonstration of Quasi-Planar Segmented-Channel MOSFET Design for Improved Scalability. *IEEE Transactions on Electron Devices*, **2012**, 59, 2273-2276	2.9	4
31	Inserted-oxide FinFET (iFinFET) design to extend CMOS scaling **2015**,		4
30	Tri-gate bulk MOSFET design for improved robustness to random dopant fluctuations **2008**,		4
29	ALD Refill of Nanometer-Scale Gaps with High-□Dielectric for Advanced CMOS Technologies. *Electrochemical and Solid-State Letters*, **2007**, 10, H257		4
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27	Sub-lithographic Patterning via Tilted Ion Implantation for Scaling Beyond the 7-nm Technology Node. *IEEE Transactions on Electron Devices*, **2017**, 64, 231-236	2.9	3
26	Study of Poly-SiGe Structural Properties for Modularly Integrated MEMS. *ECS Transactions*, **2006**, 3, 1131-1142		3
25	Study of MEM Relay Contact Design and Body-Bias Effects on on-State Resistance Stability. *Journal of Microelectromechanical Systems*, **2020**, 29, 1531-1536	2.5	3
24	Ultra-Low-Voltage Operation of MEM Relays for Cryogenic Logic Applications **2019**,		3
23	Simulation-Based Study of High-Density SRAM Voltage Scaling Enabled by Inserted-Oxide FinFET Technology. *IEEE Transactions on Electron Devices*, **2019**, 66, 1754-1759	2.9	2
22	Designing a low-voltage, high-current tunneling transistor79-116		2
21	Micro-relay reliability improvement by inkjet-printed microshell encapsulation **2013**,		2
20	Embedded Memory Capability of Four-Terminal Relay Technology. *IEEE Transactions on Electron Devices*, **2011**, 58, 891-894	2.9	2
19	SRAM design in fully-depleted SOI technology **2010**,		2

18	Low-Standby-Power Bulk MOSFET Design Using High-k Trench Isolation. *IEEE Electron Device Letters*, **2009**, 30, 1380-1382	4.4	2
17	SRAM cell design considerations for SOI technology **2009**,		2
16	Comparative Study of FinFET Versus Quasi-Planar HTI MOSFET for Ultimate Scalability. *IEEE Transactions on Electron Devices*, **2010**, 57, 3250-3256	2.9	2
15	Toward Monolithically Integrated Hybrid CMOS-NEM Circuits. *IEEE Transactions on Electron Devices*, **2021**, 68, 6430-6436	2.9	2
14	Reducing adhesion energy of micro-relay electrodes by ion beam synthesized oxide nanolayers. *APL Materials*, **2017**, 5, 036103	5.7	1
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12	. *IEEE Transactions on Electron Devices*, **2015**, 62, 2695-2699	2.9	1
11	Characterization of Nanometer-Scale Gap Formation. *Journal of the Electrochemical Society*, **2010**, 157, H94	3.9	1
10	Electrical Characterization of Etch Rate for Micro- and Nano-Scale Gap Formation. *Journal of Microelectromechanical Systems*, **2010**, 19, 1260-1263	2.5	1
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8	Tilted ion implantation of spin-coated SiARC films for sub-lithographic and two-dimensional patterning **2019**,		1
7	Cell Ratio Tuning for High-Density SRAM Voltage Scaling With Inserted-Oxide FinFETs. *IEEE Electron Device Letters*, **2016**, 37, 1539-1542	4.4	1
6	Breakdown and Healing of Tungsten-Oxide Films on Microelectromechanical Relay Contacts. *Journal of Microelectromechanical Systems*, **2022**, 1-10	2.5	0
5	Sublithographic Patterning of Spin-Coated SiARC Films Using Tilted Ion Implantation. *IEEE Transactions on Electron Devices*, **2020**, 67, 2510-2515	2.9	
4	NEMS Switch Technology **2014**, 370-389		
3	Beyond transistor scaling: alternative device structures for the terascale regime14-38		
2	Benchmarking alternative device structures for the terascale regime39-55		
1	Simulation-Based Study of Low Minimum Operating Voltage SRAM With Inserted-Oxide FinFETs and Gate-All-Around Transistors. *IEEE Transactions on Electron Devices*, **2022**, 69, 1823-1829	2.9	