Tsu-Jae King Liu

List of Publications by Year
in descending order

152 papers	5,358 citations	147726 31 h-index	102432 66 g-index
153 all docs	153 docs citations	153 times ranked	2896 citing authors

#	Article	IF	Citations
1	Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec. IEEE Electron Device Letters, 2007, 28, 743-745.	2.2	1,537
2	Demonstration of Integrated Micro-Electro-Mechanical Relay Circuits for VLSI Applications. IEEE Journal of Solid-State Circuits, 2011, 46, 308-320.	3.5	211
3	Technologies for Cofabricating MEMS and Electronics. Proceedings of the IEEE, 2008, 96, 306-322.	16.4	209
4	Study of Random Dopant Fluctuation Effects in Germanium-Source Tunnel FETs. IEEE Transactions on Electron Devices, 2011, 58, 3541-3548.	1.6	149
5	Tunnel Field Effect Transistor With Raised Germanium Source. IEEE Electron Device Letters, 2010, 31, 1107-1109.	2.2	141
6	Large-Scale SRAM Variability Characterization in 45 nm CMOS. IEEE Journal of Solid-State Circuits, 2009, 44, 3174-3192.	3.5	133
7	Study of Random Dopant Fluctuation Induced Variability in the Raised-Ge-Source TFET. IEEE Electron Device Letters, 2013, 34, 184-186.	2.2	124
8	Mechanical Computing Redux: Relays for Integrated Circuit Applications. Proceedings of the IEEE, 2010, 98, 2076-2094.	16.4	119
9	Integrated circuit design with NEM relays. , 2008, , .		103
10	4-terminal relay technology for complementary logic. , 2009, , .		93
11	Design, Optimization, and Scaling of MEM Relays for Ultra-Low-Power Digital Logic. IEEE Transactions on Electron Devices, 2011, 58, 236-250.	1.6	90
12	Gate Line Edge Roughness Model for Estimation of FinFET Performance Variability. IEEE Transactions on Electron Devices, 2009, 56, 3055-3063.	1.6	87
13	Study of Random-Dopant-Fluctuation (RDF) Effects for the Trigate Bulk MOSFET. IEEE Transactions on Electron Devices, 2009, 56, 1538-1542.	1.6	85
14	Design and reliability of a micro-relay technology for zero-standby-power digital logic applications. , 2009, , .		77
15	Nanoelectromechanical Switches for Low-Power Digital Computing. Micromachines, 2015, 6, 1046-1065.	1.4	66
16	Prospect of tunneling green transistor for 0.1V CMOS. , 2010, , .		61
17	Tri-Gate Bulk MOSFET Design for CMOS Scaling to the End of the Roadmap. IEEE Electron Device Letters, 2008, 29, 491-493.	2.2	59
18	A Comparative Study of Dopant-Segregated Schottky and Raised Source/Drain Double-Gate MOSFETs. IEEE Transactions on Electron Devices, 2008, 55, 2665-2677.	1.6	57

#	Article	IF	Citations
19	Variation Study of the Planar Ground-Plane Bulk MOSFET, SOI FinFET, and Trigate Bulk MOSFET Designs. IEEE Transactions on Electron Devices, 2011, 58, 3294-3299.	1.6	55
20	Characterization of Dynamic SRAM Stability in 45 nm CMOS. IEEE Journal of Solid-State Circuits, 2011, 46, 2702-2712.	3.5	54
21	Nano-Electro-Mechanical Nonvolatile Memory (NEMory) Cell Design and Scaling. IEEE Transactions on Electron Devices, 2008, 55, 3482-3488.	1.6	46
22	FinFET Evolution Toward Stacked-Nanowire FET for CMOS Technology Scaling. IEEE Transactions on Electron Devices, 2015, 62, 3945-3950.	1.6	46
23	Demonstration of integrated micro-electro-mechanical switch circuits for VLSI applications. , 2010, , .		45
24	Characterization of Contact Resistance Stability in MEM Relays With Tungsten Electrodes. Journal of Microelectromechanical Systems, 2012, 21, 511-513.	1.7	43
25	Mechanically modulated tunneling resistance in monolayer MoS2. Applied Physics Letters, 2013, 103, .	1.5	43
26	A New Switching Device for Printed Electronics: Inkjet-Printed Microelectromechanical Relay. Nano Letters, 2013, 13, 5355-5360.	4.5	42
27	Performance and Area Scaling Benefits of FD-SOI Technology for 6-T SRAM Cells at the 22-nm Node. IEEE Transactions on Electron Devices, 2010, 57, 1301-1309.	1.6	40
28	Perfectly Complementary Relay Design for Digital Logic Applications. IEEE Electron Device Letters, 2010, 31, 371-373.	2.2	40
29	Compact Nano-Electro-Mechanical Non-Volatile Memory (NEMory) for 3D Integration. , 2007, , .		39
30	Effectiveness of Stressors in Aggressively Scaled FinFETs. IEEE Transactions on Electron Devices, 2012, 59, 1592-1598.	1.6	39
31	ZrO₂ Ferroelectric FET for Non-volatile Memory Application. IEEE Electron Device Letters, 2019, 40, 1419-1422.	2.2	38
32	Dopant-Segregated Schottky Source/Drain Double-Gate MOSFET Design in the Direct Source-to-Drain Tunneling Regime. IEEE Transactions on Electron Devices, 2009, 56, 2016-2026.	1.6	37
33	Hybrid CMOS/BEOL-NEMS technology for ultra-low-power IC applications. , 2014, , .		36
34	Seesaw Relay Logic and Memory Circuits. Journal of Microelectromechanical Systems, 2010, 19, 1012-1014.	1.7	35
35	The relay reborn. IEEE Spectrum, 2012, 49, 40-43.	0.5	33
36	Characterization of Polycrystalline Silicon-Germanium Film Deposition for Modularly Integrated MEMS Applications. Journal of Microelectromechanical Systems, 2007, 16, 68-77.	1.7	32

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37	Impact of Body Doping and Thickness on the Performance of Germanium-Source TFETs. IEEE Transactions on Electron Devices, 2010, 57, 1710-1713.	1.6	32
38	Comparison of SOI Versus Bulk FinFET Technologies for 6T-SRAM Voltage Scaling at the 7-/8-nm Node. IEEE Transactions on Electron Devices, 2017, 64, 329-332.	1.6	32
39	Design Optimization of Multigate Bulk MOSFETs. IEEE Transactions on Electron Devices, 2013, 60, 28-33.	1.6	31
40	Adhesive Force Characterization for MEM Logic Relays With Sub-Micron Contacting Regions. Journal of Microelectromechanical Systems, 2014, 23, 198-203.	1.7	31
41	Analysis of 7/8-nm Bulk-Si FinFET Technologies for 6T-SRAM Scaling. IEEE Transactions on Electron Devices, 2016, 63, 1502-1507.	1.6	30
42	Analysis and demonstration of MEM-relay power gating. , 2010, , .		26
43	Sub-100 mV Computing With Electro-Mechanical Relays. IEEE Transactions on Electron Devices, 2017, 64, 1323-1329.	1.6	26
44	Three-Dimensional FinFET Source/Drain and Contact Design Optimization Study. IEEE Transactions on Electron Devices, 2009, 56, 1483-1492.	1.6	25
45	Simulation-Based Study of the Inserted-Oxide FinFET for Future Low-Power System-on-Chip Applications. IEEE Electron Device Letters, 2015, 36, 742-744.	2.2	25
46	Sub-50 mV NEM relay operation enabled by self-assembled molecular coating. , 2016, , .		25
47	Carrier-Mobility Enhancement via Strain Engineering in Future Thin-Body MOSFETs. IEEE Electron Device Letters, 2012, 33, 318-320.	2.2	24
48	Performance and Yield Benefits of Quasi-Planar Bulk CMOS Technology for 6-T SRAM at the 22-nm Node. IEEE Transactions on Electron Devices, 2011, 58, 1846-1854.	1.6	23
49	Four-Terminal-Relay Body-Biasing Schemes for Complementary Logic Circuits. IEEE Electron Device Letters, 2010, 31, 890-892.	2.2	21
50	Design Requirements for Steeply Switching Logic Devices. IEEE Transactions on Electron Devices, 2012, 59, 326-334.	1.6	21
51	Non-Volatile Nano-Electro-Mechanical Memory for Energy-Efficient Data Searching. IEEE Electron Device Letters, 2016, 37, 31-34.	2.2	20
52	Nanocrystal-Embedded-Insulator (NEI) Ferroelectric Field-Effect Transistor Featuring Low Operating Voltages and Improved Synaptic Behavior. IEEE Electron Device Letters, 2019, 40, 1933-1936.	2.2	20
53	Dopant-Segregated Schottky Junction Tuning With Fluorine Pre-Silicidation Ion Implant. IEEE Transactions on Electron Devices, 2010, 57, 1084-1092.	1.6	19
54	Spacer Gate Lithography for Reduced Variability Due to Line Edge Roughness. IEEE Transactions on Semiconductor Manufacturing, 2010, 23, 311-315.	1.4	19

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55	SOI TFET $I_{m ON}/I_{m OFF}$ Enhancement via Back Biasing. IEEE Transactions on Electron Devices, 2011, 58, 3283-3285.	1.6	19
56	Back-End-of-Line Nano-Electro-Mechanical Switches for Reconfigurable Interconnects. IEEE Electron Device Letters, 2020, 41, 625-628.	2.2	19
57	Scaling Limitations for Flexural Beams Used in Electromechanical Devices. IEEE Transactions on Electron Devices, 2009, 56, 688-691.	1.6	18
58	Planar GeOI TFET Performance Improvement With Back Biasing. IEEE Transactions on Electron Devices, 2012, 59, 1629-1635.	1.6	18
59	High-Mobility Ge pMOSFETs With Crystalline ZrO₂ Dielectric. IEEE Electron Device Letters, 2019, 40, 371-374.	2.2	18
60	Pull-In and Release Voltage Design for Nanoelectromechanical Field-Effect Transistors. IEEE Transactions on Electron Devices, 2009, 56, 3072-3082.	1.6	17
61	Four-Terminal Relay Design for Improved Body Effect. IEEE Electron Device Letters, 2010, 31, 515-517.	2.2	17
62	Embedded Nano-Electro-Mechanical Memory for Energy-Efficient Reconfigurable Logic. IEEE Electron Device Letters, 2016, 37, 1563-1565.	2.2	17
63	Prospects for MEM logic switch technology. , 2010, , .		16
64	Highly scaled (Lgâˆ¼56nm) gate-last Si tunnel field-effect transistors with ION>100Î¼A/Î¼m. Solid-State Electronics, 2011, 65-66, 22-27.	0.8	16
65	Design of Gate-All-Around Silicon MOSFETs for 6-T SRAM Area Efficiency and Yield. IEEE Transactions on Electron Devices, 2014, 61, 2371-2377.	1.6	16
66	Study of bending-induced strain effects on MuGFET performance. IEEE Electron Device Letters, 2006, 27, 671-673.	2.2	15
67	Multiple-Input Relay Design for More Compact Implementation of Digital Logic Circuits. IEEE Electron Device Letters, 2012, 33, 281-283.	2.2	15
68	Comparative Study of Uniform Versus Supersteep Retrograde MOSFET Channel Doping and Implications for 6-T SRAM Yield. IEEE Transactions on Electron Devices, 2013, 60, 1790-1793.	1.6	15
69	Variation-Aware Comparative Study of 10-nm GAA Versus FinFET 6-T SRAM Performance and Yield. IEEE Transactions on Electron Devices, 2014, 61, 3949-3954.	1.6	15
70	Effect of Body Biasing on the Energy-Delay Performance of Logic Relays. IEEE Electron Device Letters, 2015, 36, 862-864.	2.2	15
71	Nanomechanical Switch Designs to Overcome the Surface Adhesion Energy Limit. IEEE Electron Device Letters, 2015, 36, 963-965.	2.2	15
72	Scale-Length Assessment of the Trigate Bulk MOSFET Design. IEEE Transactions on Electron Devices, 2009, 56, 2840-2842.	1.6	14

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73	Impact of Gate Line-Edge Roughness (LER) Versus Random Dopant Fluctuations (RDF) on Germanium-Source Tunnel FET Performance. IEEE Nanotechnology Magazine, 2013, 12, 1061-1067.	1.1	14
74	Nanocrystal-Embedded-Insulator Ferroelectric Negative Capacitance FETs with Sub-kT/q Swing. IEEE Electron Device Letters, 2018, , 1-1.	2.2	14
75	Multi-input/multi-output relay design for more compact and versatile implementation of digital logic with zero leakage. , 2012, , .		13
76	Stable ruthenium-contact relay technology for low-power logic. , 2013, , .		13
77	Physically Based Modeling of Stress-Induced Variation in Nanoscale Transistor Performance. IEEE Transactions on Device and Materials Reliability, 2011, 11, 378-386.	1.5	12
78	Electromechanical Diode Cell for Cross-Point Nonvolatile Memory Arrays. IEEE Electron Device Letters, 2012, 33, 131-133.	2.2	12
79	MOSFET performance and scalability enhancement by insertion of oxygen layers. , 2012, , .		12
80	Selective Enhancement of SiO[sub 2] Etch Rate by Ar-Ion Implantation for Improved Etch Depth Control. Electrochemical and Solid-State Letters, 2007, 10, D89.	2.2	11
81	The Effect of Random Dopant Fluctuation on Specific Contact Resistivity. IEEE Transactions on Electron Devices, 2010, 57, 273-281.	1.6	11
82	Interfacial Adhesion between Rough Surfaces of Polycrystalline Silicon and Its Implications for M/NEMS Technology. Journal of Adhesion Science and Technology, 2010, 24, 2545-2556.	1.4	11
83	Reliability of MEM relays for zero leakage logic. Proceedings of SPIE, 2013, , .	0.8	11
84	Extension of Planar Bulk n-Channel MOSFET Scaling With Oxygen Insertion Technology. IEEE Transactions on Electron Devices, 2014, 61, 3345-3349.	1.6	11
85	Microelectromechanical Relay and Logic Circuit Design for Zero Crowbar Current. IEEE Transactions on Electron Devices, 2014, 61, 3296-3302.	1.6	11
86	Energy-delay performance optimization of NEM logic relay. , 2015, , .		11
87	Electron mobility enhancement in (100) oxygen-inserted silicon channel. Applied Physics Letters, 2015, 107, .	1.5	10
88	Channel Stress and Ballistic Performance Advantages of Gate-All-Around FETs and Inserted-Oxide FinFETs. IEEE Nanotechnology Magazine, 2017, 16, 209-216.	1.1	10
89	Ultra-Low-Voltage Operation of MEM Relays for Cryogenic Logic Applications. , 2019, , .		10
90	Enhanced endurance of dual-bit SONOS NVM cells using the GIDL read method. , 2008, , .		9

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91	Impact of Gate-Induced Strain on MuGFET Reliability. IEEE Electron Device Letters, 2008, 29, 916-919.	2.2	9
92	DSS MOSFET With Tunable SDE Regions by Fluorine Pre-Silicidation Ion Implant. IEEE Electron Device Letters, 2010, 31, 785-787.	2.2	9
93	Tunnel FET-based pass-transistor logic for ultra-low-power applications. , 2011, , .		9
94	There's plenty of room at the top. , 2017, , .		9
95	FinFET Performance Enhancement with Tensile Metal Gates and Strained Silicon on Insulator (sSOI) Substrate. , 2006, , .		8
96	Sub-60nm Si tunnel field effect transistors with I<inf>on</inf> >100 µA/µm. , 2010, , .		8
97	Quasi-planar bulk CMOS technology for improved SRAM scalability. Solid-State Electronics, 2011, 65-66, 184-190.	0.8	8
98	Recent progress and challenges for relay logic switch technology. , 2012, , .		8
99	Examining the Self-Efficacy of Community College STEM Majors: Factors Related to Four-Year Degree Attainment. Community College Journal of Research and Practice, 2015, 39, 1111-1124.	0.8	8
100	Inserted-oxide FinFET (iFinFET) design to extend CMOS scaling. , 2015, , .		8
101	Threshold Voltage and DIBL Variability Modeling Based on Forward and Reverse Measurements for SRAM and Analog MOSFETs. IEEE Transactions on Electron Devices, 2015, 62, 1119-1126.	1.6	8
102	Tilted ion implantation as a cost-efficient sublithographic patterning technique. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2016, 34, 040608.	0.6	8
103	Dual-Bit Gate-Sidewall Storage FinFET NVM and New Method of Charge Detection. IEEE Electron Device Letters, 2007, 28, 502-505.	2.2	7
104	Reliability of Nanoelectromechanical Nonvolatile Memory (NEMory) Cells. IEEE Electron Device Letters, 2009, 30, 269-271.	2.2	7
105	First Demonstration of Quasi-Planar Segmented-Channel MOSFET Design for Improved Scalability. IEEE Transactions on Electron Devices, 2012, 59, 2273-2276.	1.6	7
106	NEM relay design for compact, ultra-low-power digital logic circuits. , 2014, , .		7
107	Variability Study for Low-Voltage Microelectromechanical Relay Operation. IEEE Transactions on Electron Devices, 2018, 65, 1529-1534.	1.6	7
108	Toward Monolithically Integrated Hybrid CMOS-NEM Circuits. IEEE Transactions on Electron Devices, 2021, 68, 6430-6436.	1.6	7

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109	FinFET Design for Tolerance to Statistical Dopant Fluctuations. IEEE Nanotechnology Magazine, 2009, 8, 375-378.	1.1	6
110	Tri-gate bulk CMOS technology for improved SRAM scalability. , 2010, , .		6
111	pMOSFET Performance Enhancement With Strained $ hbox{Si}_{1 - x}hbox{Ge}_{x}$ Channels. IEEE Transactions on Electron Devices, 2012, 59, 1468-1474.	1.6	6
112	Fabrication of $hbox{Si}_{1 - x}hbox{Ge}_{x}/hbox{Si}$ pMOSFETs Using Corrugated Substrates for Improved $I_{m ON}$ and Reduced Layout-Width Dependence. IEEE Transactions on Electron Devices, 2013, 60, 153-158.	1.6	6
113	Designing a low-voltage, high-current tunneling transistor. , 2014, , 79-116.		6
114	Sub-lithographic Patterning via Tilted Ion Implantation for Scaling Beyond the 7-nm Technology Node. IEEE Transactions on Electron Devices, 2017, 64, 231-236.	1.6	6
115	Reducing adhesion energy of nano-electro-mechanical relay contacts by self-assembled Perfluoro (2,3-Dimethylbutan-2-ol) coating. AIP Advances, 2019, 9, 055329.	0.6	6
116	Study of Poly-SiGe Structural Properties for Modularly Integrated MEMS. ECS Transactions, 2006, 3, 1131-1142.	0.3	5
117	ALD Refill of Nanometer-Scale Gaps with High-Î¹ Dielectric for Advanced CMOS Technologies. Electrochemical and Solid-State Letters, 2007, 10, H257.	2.2	5
118	Electromechanical Diode Cell Scaling for High-Density Nonvolatile Memory. IEEE Transactions on Electron Devices, 2014, 61, 1382-1387.	1.6	5
119	Extending CMOS with negative capacitance. , 2014, , 56-76.		5
120	Study of MEM Relay Contact Design and Body-Bias Effects on on-State Resistance Stability. Journal of Microelectromechanical Systems, 2020, 29, 1531-1536.	1.7	5
121	Tri-gate bulk MOSFET design for improved robustness to random dopant fluctuations. , 2008, , .		4
122	SRAM cell design considerations for SOI technology. , 2009, , .		4
123	Raised-Source/Drain Double-Gate Transistor Design Optimization for Low Operating Power. IEEE Transactions on Electron Devices, 2013, 60, 1040-1045.	1.6	4
124	SRAM design in fully-depleted SOI technology. , 2010, , .		3
125	Embedded Memory Capability of Four-Terminal Relay Technology. IEEE Transactions on Electron Devices, 2011, 58, 891-894.	1.6	3
126	Micro-relay reliability improvement by inkjet-printed microshell encapsulation. , 2013, , .		3

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127	Cell Ratio Tuning for High-Density SRAM Voltage Scaling With Inserted-Oxide FinFETs. IEEE Electron Device Letters, 2016, 37, 1539-1542.	2.2	3
128	Simulation-Based Study of High-Density SRAM Voltage Scaling Enabled by Inserted-Oxide FinFET Technology. IEEE Transactions on Electron Devices, 2019, 66, 1754-1759.	1.6	3
129	Breakdown and Healing of Tungsten-Oxide Films on Microelectromechanical Relay Contacts. Journal of Microelectromechanical Systems, 2022, 31, 265-274.	1.7	3
130	Simulation-Based Study of Low Minimum Operating Voltage SRAM With Inserted-Oxide FinFETs and Gate-All-Around Transistors. IEEE Transactions on Electron Devices, 2022, 69, 1823-1829.	1.6	3
131	Low-Standby-Power Bulk MOSFET Design Using High-k Trench Isolation. IEEE Electron Device Letters, 2009, 30, 1380-1382.	2.2	2
132	Comparative Study of FinFET Versus Quasi-Planar HTI MOSFET for Ultimate Scalability. IEEE Transactions on Electron Devices, 2010, 57, 3250-3256.	1.6	2
133	Fabrication of segmented-channel MOSFETs for reduced short-channel effects. , 2011, , .		2
134	Why hybridize NEMS with CMOS?. , 2014, , .		2
135	Experimental Studies of Contact Detachment Delay in Microrelays for Logic Applications. IEEE Transactions on Electron Devices, 2015, 62, 2695-2699.	1.6	2
136	Reducing adhesion energy of micro-relay electrodes by ion beam synthesized oxide nanolayers. APL Materials, 2017, 5, 036103.	2.2	2
137	Simulation-Based Study of High-Permittivity Inserted-Oxide FinFET With Low-Permittivity Inner Spacers. IEEE Transactions on Electron Devices, 2021, 68, 5529-5534.	1.6	2
138	Study of DC-Driven MEM Relay Oscillators for Implementation of Ising Machines. , 2021, , .		2
139	Characterization of Nanometer-Scale Gap Formation. Journal of the Electrochemical Society, 2010, 157, H94.	1.3	1
140	Electrical Characterization of Etch Rate for Micro- and Nano-Scale Gap Formation. Journal of Microelectromechanical Systems, 2010, 19, 1260-1263.	1.7	1
141	Mechanical switches. , 0, , 263-298.		1
142	Tilted ion implantation of spin-coated SiARC films for sub-lithographic and two-dimensional patterning. , 2019, , .		1
143	3D Integrated CMOS-NEM Systems: Enabling Next-Generation Computing Technology. , 2021, , .		1
144	Steep-subthreshold-slope devices on SOI. , 2011, , .		0

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145	Collaborative research on emerging technologies and design. Proceedings of SPIE, 2011, , .	0.8	0
146	Quasi-Planar Tri-gate (QPT) bulk CMOS technology for single-port SRAM application. , 2012, , .		0
147	A dual-voltage hybrid NEMS-CMOS low-power scheme. , 2014, , .		0
148	Oxygen-inserted SegFET: A candidate for 10-nm node system-on-chip applications. , 2014, , .		0
149	Beyond transistor scaling: alternative device structures for the terascale regime. , 0, , 14-38.		0
150	Benchmarking alternative device structures for the terascale regime. , 0, , 39-55.		0
151	Sublithographic Patterning of Spin-Coated SiARC Films Using Tilted Ion Implantation. IEEE Transactions on Electron Devices, 2020, 67, 2510-2515.	1.6	0
152	Extending the era of Moore's Law. , 2017, , .		0