Chang-Chih Chen

List of Publications by Year
in descending order

22	212	1307594 7	1281871 11
papers	citations	h-index	g-index

22	22	22	96
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	System-level variation-aware aging simulator using a unified novel gate-delay model for bias temperature instability, hot carrier injection, and gate oxide breakdown. Microelectronics Reliability, 2015, 55, 1334-1340.	1.7	25
2	System-Level Modeling and Microprocessor Reliability Analysis for Backend Wearout Mechanisms. , 2013, , .		22
3	SRAM stability analysis for different cache configurations due to Bias Temperature Instability and Hot Carrier Injection. , 2016, , .		18
4	System-Level Modeling of Microprocessor Reliability Degradation Due to Bias Temperature Instability and Hot Carrier Injection. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2712-2725.	3.1	17
5	Comprehensive reliability and aging analysis on SRAMs within microprocessor systems. Microelectronics Reliability, 2015, 55, 1290-1296.	1.7	15
6	Comprehensive Reliability-Aware Statistical Timing Analysis Using a Unified Gate-Delay Model for Microprocessors. IEEE Transactions on Emerging Topics in Computing, 2018, 6, 219-232.	4.6	15
7	System-level modeling and reliability analysis of microprocessor systems. , 2013, , .		13
8	Backend dielectric chip reliability simulator for complex interconnect geometries. , 2012, , .		11
9	Accurate standard cell characterization and statistical timing analysis using multivariate adaptive regression splines. , 2015, , .		10
10	Built-In Self-Test Methodology With Statistical Analysis for Electrical Diagnosis of Wearout in a Static Random Access Memory Array. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2521-2534.	3.1	10
11	A comparative study of wearout mechanisms in state-of-art microprocessors. , 2012, , .		8
12	Processor-level reliability simulator for time-dependent gate dielectric breakdown. Microprocessors and Microsystems, 2015, 39, 950-960.	2.8	8
13	Impact of NBTI/PBTIon SRAMs within microprocessor systems: Modeling, simulation, and analysis. Microelectronics Reliability, 2013, 53, 1183-1188.	1.7	7
14	Backend Dielectric Reliability Full Chip Simulator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1750-1762.	3.1	7
15	SRAM Stability Analysis and Performanceâ€“Reliability Tradeoff for Different Cache Configurations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 620-633.	3.1	7
16	Backend dielectric reliability simulator for microprocessor system. Microelectronics Reliability, 2012, 52, 1953-1959.	1.7	4
17	Diagnosis of resistive-open defects due to electromigration and stress-induced voiding in an SRAM array. , 2014, , .		4
18	Simulation of system backend dielectric reliability. Microelectronics Journal, 2014, 45, 1327-1334.	2.0	4

#	Article	IF	Citations
19	Estimation of remaining life using embedded SRAM for wearout parameter extraction. , 2015, , .		3
20	MBIST and statistical hypothesis test for time dependent dielectric breakdowns due to GOBD vs. BTDDB in an SRAM array. , 2015, , .		2
21	System-level modeling of microprocessor reliability degradation due to TDDB. , 2014, , .		1
22	Reliability and Aging Analysis on SRAMs Within Microprocessor Systems. , 2018, , .		1