Sung Kyu Lim

List of Publications by Citations

157 papers	1,901 citations	24 h-index	36 g-index
176 ext. papers	2,377 ext. citations	2.3 avg, IF	4.96 L-index

#	Paper	IF	Citations
157	A study of Through-Silicon-Via impact on the 3D stacked IC layout **2009**,		106
156	3D-MAPS: 3D Massively parallel processor with stacked memory **2012**,		84
155	TSV stress aware timing analysis with applications to 3D-IC layout optimization **2010**,		72
154	Multiobjective Microarchitectural Floorplanning for 2-D and 3-D ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 38-52	2.5	67
153	Fast and Accurate Analytical Modeling of Through-Silicon-Via Capacitive Coupling. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2011**, 1, 168-180	1.7	54
152	Edge separability-based circuit clustering with application to multilevel circuit partitioning. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2004**, 23, 346-357	2.5	50
151	Design method and test structure to characterize and repair TSV defect induced signal degradation in 3D system **2010**,		47
150	Stress-driven 3D-IC placement with TSV keep-out zone and regularity study **2010**,		47
149	TSV stress-aware full-chip mechanical reliability analysis and optimization for 3D IC. *Communications of the ACM*, **2014**, 57, 107-115	2.5	46
148	Study of Through-Silicon-Via Impact on the 3-D Stacked IC Layout. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 862-874	2.6	44
147	Pre-Bond and Post-Bond Test and Signal Recovery Structure to Characterize and Repair TSV Defect Induced Signal Degradation in 3-D System. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2011**, 1, 1718-1727	1.7	42
146	Design and Analysis of 3D-MAPS (3D Massively Parallel Processor with Stacked Memory). *IEEE Transactions on Computers*, **2015**, 64, 112-125	2.5	41
145	High-density integration of functional modules using monolithic 3D-IC technology **2013**,		37
144	Through-silicon-via management during 3D physical design: When to add and how many? **2010**,		35
143	TSV Stress-Aware Full-Chip Mechanical Reliability Analysis and Optimization for 3-D IC. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1194-1207	2.5	30
142	Reliable 3-D Clock-Tree Synthesis Considering Nonlinear Capacitive TSV Model With Electrical–Thermal–Mechanical Coupling. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 1734-1747	2.5	28
141	TSV-Based 3-D ICs: Design Methods and Tools. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1593-1619	2.5	27

140	Placement-Driven Partitioning for Congestion Mitigation in Monolithic 3D IC Designs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 540-553	2.5	27
139	Silicon Effect-Aware Full-Chip Extraction and Mitigation of TSV-to-TSV Coupling. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 1900-1913	2.5	27
138	Ultra-high density 3D SRAM cell designs for monolithic 3D integration **2012**,		26
137	Shrunk-2-D: A Physical Design Methodology to Build Commercial-Quality Monolithic 3-D ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1716-1724	2.5	25
136	Low-Power Clock Tree Design for Pre-Bond Testing of 3-D Stacked ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 732-745	2.5	25
135	Improvement of memory performance by high temperature annealing of the Al2O3 blocking layer in a charge-trap type flash memory device. *Applied Physics Letters*, **2010**, 96, 222902	3.4	25
134	Placement for large-scale floating-gate field-programable analog arrays. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2006**, 14, 906-910	2.6	24
133	Ultrahigh Density Logic Designs Using Monolithic 3-D Integration. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 1892-1905	2.5	22
132	A study of IR-drop noise issues in 3D ICs with through-silicon-vias **2010**,		22
131	TSV-Aware Interconnect Distribution Models for Prediction of Delay and Power Consumption of 3-D Stacked ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 1384-1395	2.5	21
130	Distributed TSV Topology for 3-D Power-Supply Networks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 2066-2079	2.6	21
129	Block-level 3D IC design with through-silicon-via planning **2012**,		20
128	Analysis of TSV-to-TSV coupling with high-impedance termination in 3D ICs **2011**,		20
127	3D Floorplanning with Thermal Vias **2006**,		20
126	Design for manufacturability and reliability for TSV-based 3D ICs **2012**,		19
125	Design challenges and solutions for ultra-high-density monolithic 3D ICs **2014**,		18
124	Co-Optimization and Analysis of Signal, Power, and Thermal Interconnects in 3-D ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 1635-1648	2.5	17
123	Methodology to determine the impact of linewidth variation on chip scale copper/low-k backend dielectric breakdown. *Microelectronics Reliability*, **2010**, 50, 1341-1346	1.2	17

122	Design Quality Trade-Off Studies for 3-D ICs Built With Sub-Micron TSVs and Future Devices. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2012**, 2, 240-248	5.2	16
121	A study of stacking limit and scaling in 3D ICs: an interconnect perspective **2009**,		16
120	Backend low-k TDDB chip reliability simulator **2011**,		16
119	Full-Chip Signal Integrity Analysis and Optimization of 3-D ICs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 1636-1648	2.6	14
118	Exploiting Die-to-Die Thermal Coupling in 3-D IC Placement. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 2145-2155	2.6	13
117	Slew-aware buffer insertion for through-silicon-via-based 3D ICs **2012**,		13
116	Impact of size effects in local interconnects for future technology nodes: A study based on full-chip layouts **2014**,		12
115	Impact of nano-scale through-silicon vias on the quality of today and future 3D IC designs **2011**,		12
114	Noise-Direct: A Technique for Power Supply Noise Aware Floorplanning Using Microarchitecture Profiling **2007**,		12
113	Adaptive Regression-Based Thermal Modeling and Optimization for Monolithic 3-D ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 1707-1720	2.5	11
112	Power, performance, and cost comparisons of monolithic 3D ICs and TSV-based 3D ICs **2015**,		11
111	Electromigration Study for Multiscale Power/Ground Vias in TSV-Based 3-D ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 1873-1885	2.5	11
110	Whitespace redistribution for thermal via insertion in 3D stacked ICs **2007**,		11
109	. *IEEE Transactions on Electron Devices*, **2016**, 1-4	2.9	10
108	Impact of Mechanical Stress on the Full Chip Timing for Through-Silicon-Via-based 3-D ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 905-917	2.5	10
107	Chip/Package Mechanical Stress Impact on 3-D IC Reliability and Mobility Variations. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 1694-1707	2.5	10
106	Designing 3D test wrappers for pre-bond and post-bond test of 3D embedded cores **2011**,		10
105	Routing optimization of multi-modal interconnects in 3D ICs **2009**,		10

104	Analysis and Modeling of DC Current Crowding for TSV-Based 3-D Connections and Power Integrity. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2014**, 4, 123-133	1.7	9
103	Signal integrity analysis and optimization for 3D ICs **2011**,		9
102	Power-supply-network design in 3D integrated systems **2011**,		9
101	Chip/package co-analysis of thermo-mechanical stress and reliability in TSV-based 3D ICs **2012**,		9
100	Analysis of DC current crowding in through-silicon-vias and its impact on power integrity in 3D ICs **2012**,		9
99	Timing analysis and optimization for 3D stacked multi-core microprocessors **2010**,		9
98	Rapid Prototyping of Large-scale Analog Circuits With Field Programmable Analog Array **2007**,		9
97	Wire congestion and thermal aware 3D global placement		9
96	A Floorplan-Aware Dynamic Inductive Noise Controller for Reliable Processor Design. *Microarchitecture (MICRO), Proceedings of the Annual International Symposium on*, **2006**,		9
95	Evaluating Chip-Level Impact of Cu/Low- $kappa $ Performance Degradation on Circuit Performance at Future Technology Nodes. *IEEE Transactions on Electron Devices*, **2015**, 62, 940-946	2.9	8
94	Analysis and Design of Energy and Slew Aware Subthreshold Clock Systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 1349-1358	2.5	8
93	Scan chain and power delivery network synthesis for pre-bond test of 3D ICs **2011**,		8
92	Backend dielectric chip reliability simulator for complex interconnect geometries **2012**,		8
91	Microarchitectural Floorplanning Under Performance and Thermal Tradeoff **2006**,		8
90	Effective thermal via and decoupling capacitor insertion for 3D system-on-package		8
89	Heterogeneous Mixed-Signal Monolithic 3-D In-Memory Computing Using Resistive RAM. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 386-396	2.6	8
88	Entropy Production-Based Full-Chip Fatigue Analysis: From Theory to Mobile Applications. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 84-95	2.5	7
87	TSV Stress-Aware ATPG for 3D Stacked ICs **2012**,		7

86	Scan test of die logic in 3D ICs using TSV probing **2012**,		7
85	Co-design of reliable signal and power interconnects in 3D stacked ICs **2009**,		7
84	Optical Routing for 3-D System-On-Package. *IEEE Transactions on Components and Packaging Technologies*, **2007**, 30, 805-812		7
83	Reliability-aware floorplanning for 3D circuits		7
82	Architecture, Chip, and Package Codesign Flow for Interposer-Based 2.5-D Chiplet Integration Enabling Heterogeneous IP Reuse. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 2424-2437	2.6	7
81	Backend Dielectric Reliability Full Chip Simulator. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 1750-1762	2.6	6
80	Full Chip Impact Study of Power Delivery Network Designs in Gate-Level Monolithic 3-D ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 992-1003	2.5	6
79	Variation-Aware Clock Network Design Methodology for Ultralow Voltage (ULV) Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1222-1234	2.5	6
78	A study of signal integrity issues in through-silicon-via-based 3D ICs **2010**,		6
77	Buffered clock tree sizing for skew minimization under power and thermal budgets **2010**,		6
76	A study of TSV variation impact on power supply noise **2011**,		6
75	Thermal optimization in multi-granularity multi-core floorplanning **2009**,		6
74	Thermal-aware steiner routing for 3D stacked ICs. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, **2007**,		6
73	Multi-objective module placement for 3-D system-on-package. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2006**, 14, 553-557	2.6	6
72	Parasitic Extraction for Heterogeneous Face-to-Face Bonded 3-D ICs. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2017**, 7, 912-924	1.7	5
71	Impact and Design Guideline of Monolithic 3-D IC at the 7-nm Technology Node. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2118-2129	2.6	5
70	Ultralow Power Circuit Design With Subthreshold/Near-Threshold 3-D IC Technologies. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2015**, 5, 980-990	1.7	5
69	Compact-2D: A Physical Design Methodology to Build Two-Tier Gate-Level 3-D ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 1151-1164	2.5	5

68	Probe-Pad Placement for Prebond Test of 3-D ICs. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2016**, 6, 637-644	1.7	5
67	Design and Analysis of a Stochastic Flash Analog-to-Digital Converter in 3D IC technology for integration with ultrasound transducer array. *Microelectronics Journal*, **2016**, 48, 39-49	1.8	5
66	Multi-TSV and E-Field Sharing Aware Full-chip Extraction and Mitigation of TSV-to-Wire Coupling. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 1964-1976	2.5	5
65	Design quality tradeoff studies for 3D ICs built with nano-scale TSVs and devices **2012**,		5
64	Tier Adaptive Body Biasing: A Post-Silicon Tuning Method to Minimize Clock Skew Variations in 3-D ICs. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2013**, 3, 1720-1730	1.7	5
63	Net and pin distribution for 3D package global routing		5
62	Thermal and Crosstalk-Aware Physical Design for 3D System-On-Package		5
61	Performance, Power, and Area of Standard Cells in Sub 3 nm Node Using Buried Power Rail. *IEEE Transactions on Electron Devices*, **2022**, 1-6	2.9	5
60	Tier Degradation of Monolithic 3-D ICs: A Power Performance Study at Different Technology Nodes. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1265-1273	2.5	4
59	RTL-to-GDS Tool Flow and Design-for-Test Solutions for Monolithic 3D ICs **2019**,		4
58	Heterogeneous 3D Integration for a RISC-V System With STT-MRAM. *IEEE Computer Architecture Letters*, **2020**, 19, 51-54	1.8	4
57	Fine-Grained 3-D IC Partitioning Study With a Multicore Processor. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2015**, 5, 1393-1401	1.7	4
56	Fast delay estimation with buffer insertion for through-silicon-via-based 3D interconnects **2012**,		4
55	Transition delay fault testing of 3D ICs with IR-drop study **2012**,		4
54	Block-level designs of die-to-wafer bonded 3D ICs and their design quality tradeoffs **2013**,		4
53	Impact of through-silicon-via scaling on the wirelength distribution of current and future 3D ICs **2011**,		4
52	TSV density-driven global placement for 3D stacked ICs **2011**,		4
51	Optical Routing for 3D System-On-Package **2006**,		4

50	Decoupling-Capacitor Planning and Sizing for Noise and Leakage Reduction. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 2023-2034	2.5	4
49	Retiming-based timing analysis with an application to mincut-based global placement. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2004**, 23, 1684-1692	2.5	4
48	Cross-Domain Optimization of Ferroelectric Parameters for Negative Capacitance TransistorsPart I: Constant Supply Voltage. *IEEE Transactions on Electron Devices*, **2020**, 67, 365-370	2.9	4
47	Antiferroelectric negative capacitance from a structural phase transition in zirconia.. *Nature Communications*, **2022**, 13, 1228	17.4	4
46	Residual Stress and Pop-Out Simulation for TSVs and Contacts in Via-Middle Process. *IEEE Transactions on Semiconductor Manufacturing*, **2017**, 30, 143-154	2.6	3
45	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 888-898	2.6	3
44	Simulation of system backend dielectric reliability. *Microelectronics Journal*, **2014**, 45, 1327-1334	1.8	3
43	Backend dielectric reliability simulator for microprocessor system. *Microelectronics Reliability*, **2012**, 52, 1953-1959	1.2	3
42	Mechanism of Date Retention Improvement by High Temperature Annealing of Al2O3Blocking Layer in Flash Memory Device. *Japanese Journal of Applied Physics*, **2011**, 50, 04DD07	1.4	3
41	A fine-grained co-simulation methodology for IR-drop noise in silicon interposer and TSV-based 3D IC **2011**,		3
40	Global bus route optimization with application to microarchitectural design exploration **2008**,		3
39	Traffic: a novel geometric algorithm for fast wire-optimized floorplanning. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2006**, 25, 1075-1086	2.5	3
38	Profile-guided microarchitectural floor planning for deep submicron processor design. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2006**, 25, 1289-1300	2.5	3
37	A global router for system-on-package targeting layer and crosstalk minimization		3
36	Mechanism of Date Retention Improvement by High Temperature Annealing of Al2O3Blocking Layer in Flash Memory Device. *Japanese Journal of Applied Physics*, **2011**, 50, 04DD07	1.4	3
35	Parameter Extraction and Power/Performance Analysis of Monolithic 3-D Inverter (M3INV). *IEEE Transactions on Electron Devices*, **2019**, 66, 1006-1011	2.9	3
34	. *IEEE Transactions on Electromagnetic Compatibility*, **2021**, 63, 246-258	2	3
33	Design and analysis of 3D IC-based low power stereo matching processors **2013**,		2

32	Stacking integration methodologies in 3D IC for 3D ultrasound image processing application: A stochastic flash ADC design case study **2015**,		2
31	3D IC-package-board co-analysis using 3D EM simulation for mobile applications **2013**,		2
30	Co-design of signal, power, and thermal distribution networks for 3D ICs **2009**,		2
29	Module placement for power supply noise and wire congestion avoidance in 3D packaging		2
28	Wire-driven microarchitectural design space exploration		2
27	Modeling and Benchmarking Back End Of The Line Technologies on Circuit Designs at Advanced Nodes **2020**,		2
26	Optimal Ferroelectric Parameters for Negative Capacitance Field-Effect Transistors Based on Full-Chip Implementations—Part II: Scaling of the Supply Voltage. *IEEE Transactions on Electron Devices*, **2020**, 67, 371-376	2.9	2
25	Design Flow for Active Interposer-Based 2.5-D ICs and Study of RISC-V Architecture With Secure NoC. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2020**, 10, 2047-2060	1.7	2
24	Electrical Coupling and Simulation of Monolithic 3D Logic Circuits and Static Random Access Memory. *Micromachines*, **2019**, 10,	3.3	1
23	The Impact of 3D Stacking and Technology Scaling on the Power and Area of Stereo Matching Processors. *Sensors*, **2017**, 17,	3.8	1
22	Fast bidirectional shortest path on GPU. *IEICE Electronics Express*, **2016**, 13, 20160036-20160036	0.5	1
21	Chain-Based Approach for Fast Through-Silicon-Via Coupling Delay Estimation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 1178-1182	2.6	1
20	On diagnosable and tunable 3D clock network design for lifetime reliability enhancement **2015**,		1
19	Test-TSV estimation during 3D-IC partitioning **2013**,		1
18	Reliability and performance-aware 3D SRAM design **2011**,		1
17	Hierarchical placement for large-scale FPAA		1
16	Statistical Bellman-Ford algorithm with an application to retiming		1
15	Placement for configurable dataflow architecture		1

14	Machine Learning Based Variation Modeling and Optimization for 3D ICs. *Journal of Information and Communication Convergence Engineering*, **2016**, 14, 258-267		1
13	Chiplet/Interposer Co-Design for Power Delivery Network Optimization in Heterogeneous 2.5D ICs. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2021**, 1-1	1.7	1
12	Interdie Coupling Extraction and Physical Design Optimization for Face-to-Face 3-D ICs. *IEEE Nanotechnology Magazine*, **2018**, 17, 634-644	2.6	1
11	In-growth test for monolithic 3D integrated SRAM **2018**,		1
10	A Compute-in-Memory Hardware Accelerator Design with Back-end-of-line (BEOL) Transistor based Reconfigurable Interconnect. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2022**, 1-1	5.2	1
9	Impact of irregular geometries on low-k dielectric breakdown. *Microelectronics Reliability*, **2011**, 51, 1582-1586	1.2	0
8	Design Automation and Test Solutions for Monolithic 3D ICs. *ACM Journal on Emerging Technologies in Computing Systems*, **2022**, 18, 1-49	1.7	0
7	A COTS-Based Novel 3-D DRAM Memory Cube Architecture for Space Applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 2055-2068	2.6	0
6	Profile-Driven Instruction Mapping for Dataflow Architectures. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2006**, 25, 3017-3025	2.5	
5	Clock Delivery Network Design and Analysis for Interposer-Based 2.5-D Heterogeneous Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 605-616	2.6	
4	An Effective Block Pin Assignment Approach for Block-Level Monolithic 3-D ICs. *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, **2021**, 7, 26-34	2.4	
3	Design-aware Partitioning-based 3D IC Design Flow with 2D Commercial Tools. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	
2	Power Supply Noise-Aware At-Speed Delay Fault Testing of Monolithic 3-D ICs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 1-14	2.6	
1	Monolithic 3D Inverter with Interface Charge: Parameter Extraction and Circuit Simulation. *Applied Sciences (Switzerland)*, **2021**, 11, 12151	2.6	