Julien Schmaltz

List of Publications by Year
in descending order

20 papers	213 citations	1307594 7 h-index	1474206 9 g-index
20 all docs	20 docs citations	20 times ranked	80 citing authors

#	Article	IF	Citations
1	A Decision Procedure for Deadlock-Free Routing in Wormhole Networks. IEEE Transactions on Parallel and Distributed Systems, 2014, 25, 1935-1944.	5.6	14
2	Easy Formal Specification and Validation of Unbounded Networks-on-Chips Architectures. ACM Transactions on Design Automation of Electronic Systems, 2012, 17, 1-28.	2.6	12
3	Automatic generation of deadlock detection algorithms for a family of microarchitecture description languages of communication fabrics. , 2012, , .		0
4	A formally verified deadlock-free routing function in a fault-tolerant NoC architecture. , 2012, , .		3
5	Proof Pearl: A Formal Proof of Dally and Seitzâ€™ Necessary and Sufficient Condition for Deadlock-Free Routing in Interconnection Networks. Journal of Automated Reasoning, 2012, 48, 419-439.	1.4	5
6	A Comment on â€œA Necessary and Sufficient Condition for Deadlock-Free Adaptive Routing in Wormhole Networksâ€• IEEE Transactions on Parallel and Distributed Systems, 2011, 22, 1775-1776.	5.6	17
7	On Necessary and Sufficient Conditions for Deadlock-Free Routing in Wormhole Networks. IEEE Transactions on Parallel and Distributed Systems, 2011, 22, 2022-2032.	5.6	25
8	A Fast and Verified Algorithm for Proving Store-and-Forward Networks Deadlock-Free. , 2011, , .		5
9	Formal specification of networks-on-chips: deadlock and evacuation. , 2010, , .		9
10	A Formal Proof of a Necessary and Sufficient Condition for Deadlock-Free Adaptive Networks. Lecture Notes in Computer Science, 2010, , 67-82.	1.3	3
11	Formal validation of deadlock prevention in networks-on-chips. , 2009, , .		3
12	Towards a formally verified network-on-chip. , 2009, , .		3
13	A Formal Approach to the Verification of Networks on Chip. Eurasip Journal on Embedded Systems, 2009, 2009, 548324.	1.2	23
14	A functional formalization of on chip communications. Formal Aspects of Computing, 2008, 20, 241-258.	1.8	16
15	Executable formal specification and validation of NoC communication infrastructures. , 2008, , .		12
16	A Formal Model of Clock Domain Crossing and Automated Verification of Time-Triggered Hardware. , 2007, , .		13
17	A Generic Model for Formally Verifying NoC Communication Architectures: A Case Study. , 2007, , .		23
18	Towards a formal theory of on chip communications in the ACL2 logic. , 2006, , .		15

#	Article	IF	Citations
19	A Generic Network on Chip Model. Lecture Notes in Computer Science, 2005, , 310-325.	1.3	8
20	A formalisation of XMAS. Electronic Proceedings in Theoretical Computer Science, EPTCS, 0, 114, 111-126.	0.8	4