Tsuyoshi Isshiki

List of Publications by Year
in descending order

43 papers	157 citations	1937685 4 h-index	1720034 7 g-index
43 all docs	43 docs citations	43 times ranked	120 citing authors

#	Article	IF	Citations
1	Speaker Recognition Using LPC, MFCC, ZCR Features with ANN and SVM Classifier for Large Input Database. , 2019, , .		30
2	Trace-driven workload simulation method for Multiprocessor System-On-Chips. , 2009, , .		19
3	Optimized Communication and Synchronization for Embedded Multiprocessors Using ASIP Methodology. IPSJ Transactions on System LSI Design Methodology, 2012, 5, 118-132.	0.8	14
4	SIFT-based algorithm for fingerprint authentication on smartphone. , 2015, , .		13
5	Neural network based bed posture classification enhanced by Bayesian approach. , 2017, , .		9
6	High Voltage Transmission Tower Detection and Tracking in Aerial Video Sequence using Object-Based Image Classification. , 2018, , .		8
7	A Low-Cost and Energy-Efficient Multiprocessor System-on-Chip for UWB MAC Layer. IEICE Transactions on Information and Systems, 2012, E95.D, 2027-2038.	0.7	6
8	Speaker Recognition using fusion of features with Feedforward Artificial Neural Network and Support Vector Machine. , 2020, , .		6
9	A Multi-Temporal Convolutional Autoencoder Neural Network for Cloud Removal in Remote Sensing Images. , 2018, , .		5
10	A Reconfigurable High Performance ASIP Engine for Image Signal Processing. , 2012, , .		4
11	Narrow Fingerprint Sensor Verification with Template Updating Technique. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2012, E95-A, 346-353.	0.3	4
12	Efficient Synchronization for Distributed Embedded Multiprocessors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 779-783.	3.1	4
13	A High Level Design of Reconfigurable and High-Performance ASIP Engine for Image Signal Processing. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2012, E95.A, 2373-2383.	0.3	4
14	A Novel Fingerprint SoC with Bit Serial FPGA Engine. IPSJ Digital Courier, 2005, 1, 226-233.	0.3	3
15	Underwater positioning systems for underwater robots using trilateration algorithm. , 2015, , .		3
16	Small Area Fingerprint Verification using Deep Convolutional Neural Network. , 2020, , .		3
17	Dalvik Bytecode Acceleration Using Fetch/Decode Hardware Extension. Journal of Information Processing, 2015, 23, 118-130.	0.4	2
18	Online Detection of Spoof Fingers for Smartphone-Based Applications. , 2015, , .		2

#	Article	IF	Citations
19	An efficient embedded processor for object detection using ASIP methodology. , 2016, , .		2
20	Hybrid sharedâ€memory and messageâ€passing multiprocessor systemâ€onâ€chip for UWB MAC layer. IET Computers and Digital Techniques, 2017, 11, 8-15.	1.2	2
21	Hybrid Minutiae Descriptor for Narrow Fingerprint Verification. IEICE Transactions on Information and Systems, 2017, E100.D, 546-555.	0.7	2
22	High Voltage Transmission Tower Identification in an Aerial Video Sequence using Object-Based Image Classification with Geometry Information. , 2018, , .		2
23	Improving Relocalization in Visual SLAM by using Object Detection. , 2022, , .		2
24	Practical Orientation Field Estimation for Embedded Fingerprint Recognition Systems. IEICE Transactions on Information and Systems, 2011, E94-D, 1792-1799.	0.7	1
25	Flexible and High Performance ASIPs for Pixel Level Image Processing and Two Dimensional Image Processing. Journal of Information Processing, 2013, 21, 552-562.	0.4	1
26	A design method for real-time image denoising circuit using High-Level Synthesis. , 2016, , .		1
27	Design of an efficient ASIP-based processor for object detection using AdaBoost algorithm. , 2016, , .		1
28	HOG-Based Object Detection Processor Design Using ASIP Methodology. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2017, E100.A, 2972-2984.	0.3	1
29	ROS-Based Mobile Robot Pose Planning for a Good View of an Onboard Camera using Costmap. , 2019, , .		1
30	Scalable Hardware Architecture for fast Gradient Boosted Tree Training. IPSJ Transactions on System LSI Design Methodology, 2021, 14, 11-20.	0.8	1
31	Unique Fingerprint-Image-Generation Algorithm for Line Sensors. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2011, E94-A, 781-788.	0.3	1
32	A reconfigurable ASIP-based approach for high performance image signal processing. , 2012, , .		0
33	Dalvik bytecode acceleration using Fetch/Decode Hardware Extension with hybrid Execution. , 2014, , .		0
34	A Method of Software Development Tool and Hardware Generation for ASIP with a Co-processor based on the Derivative ASIP Approach. Journal of Information Processing, 2014, 22, 131-141.	0.4	0
35	Retargeting Derivative-ASIP with Assembly Converter Tool. IEICE Transactions on Information and Systems, 2014, E97.D, 1188-1195.	0.7	0
36	Efficient Design Exploration Framework of SW/HW Systems Based on Tightly-coupled Thread Model. IPSJ Transactions on System LSI Design Methodology, 2015, 8, 38-50.	0.8	0

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37	An investment decision support tool for horticulture with an adaptive energy management system. , 2015, , .		0
38	C-based RTL design method for circuit switched network on chips. , 2015, , .		0
39	A Fast Trace Aware Statistical Based Prediction Model with Burst Traffic Modeling for Contention Stall in A Priority Based MPSoC Bus. IPSJ Transactions on System LSI Design Methodology, 2016, 9, 37-48.	0.8	0
40	An Accurate and Fast Trace-aware Performance Estimation Model For Prioritized MPSoC Bus With Multiple Interfering Bus-Masters. IPSJ Transactions on System LSI Design Methodology, 2017, 10, 13-27.	0.8	0
41	Design of an Application Specific Instruction Set Processor for Real-Time Object Detection Using AdaBoost Algorithm. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2017, E100.A, 1384-1395.	0.3	0
42	Orientation Field Estimation for Embedded Fingerprint Authentication System. IEICE Transactions on Information and Systems, 2010, E93-D, 1918-1926.	0.7	0
43	Register-Based Process Virtual Machine Acceleration Using Hardware Extension with Hybrid Execution. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2015, E98.A, 2505-2518.	0.3	0