

Yang Sun

List of Publications by Year in descending order

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22
papers

470
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1684188

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2053705

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23
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23
times ranked

298
citing authors

| # | ARTICLE | IF | CITATIONS |
|----|---|-----|-----------|
| 1 | VLSI Architecture for Layered Decoding of QC-LDPC Codes With High Circulant Weight. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1960-1964. | 3.1 | 22 |
| 2 | Parallel nonbinary LDPC decoding on GPU. , 2012, , . | | 13 |
| 3 | High-Throughput Soft-Output MIMO Detector Based on Path-Preserving Trellis-Search Algorithm. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1235-1247. | 3.1 | 18 |
| 4 | Low complexity scalable MIMO sphere detection through antenna detection reordering. Analog Integrated Circuits and Signal Processing, 2012, 73, 463-472. | 1.4 | 0 |
| 5 | Trellis-Search Based Soft-Input Soft-Output MIMO Detector: Algorithm and VLSI Architecture. IEEE Transactions on Signal Processing, 2012, 60, 2617-2627. | 5.3 | 24 |
| 6 | High-throughput Contention-Free concurrent interleaver architecture for multi-standard turbo decoder. , 2011, , . | | 7 |
| 7 | GPU accelerated scalable parallel decoding of LDPC codes. , 2011, , . | | 15 |
| 8 | A Flexible LDPC/Turbo Decoder Architecture. Journal of Signal Processing Systems, 2011, 64, 1-16. | 2.1 | 27 |
| 9 | Implementation of a High Throughput Soft MIMO Detector on GPU. Journal of Signal Processing Systems, 2011, 64, 123-136. | 2.1 | 36 |
| 10 | Multi-layer parallel decoding algorithm and vlsi architecture for quasi-cyclic LDPC codes. , 2011, , . | | 31 |
| 11 | Low-complexity and high-performance soft MIMO detection based on distributed M-algorithm through trellis-diagram. , 2010, , . | | 4 |
| 12 | Implementation of a 3GPP LTE turbo decoder accelerator on GPU. , 2010, , . | | 29 |
| 13 | Scalable and low power LDPC decoder design using high level algorithmic synthesis. , 2009, , . | | 15 |
| 14 | FPGA prototyping of a high data rate LTE uplink baseband receiver. , 2009, , . | | 10 |
| 15 | A GPU implementation of a real-time MIMO detector. , 2009, , . | | 23 |
| 16 | Reconfigurable real-time MIMO detector on GPU. , 2009, , . | | 16 |
| 17 | Unified decoder architecture for LDPC/turbo codes. , 2008, , . | | 11 |
| 18 | A low-power 1-Gbps reconfigurable LDPC decoder design for multiple 4G wireless standards. , 2008, , . | | 24 |

| # | ARTICLE | IF | CITATIONS |
|----|---|----|-----------|
| 19 | A new MIMO detector architecture based on a Forward-Backward trellis algorithm. , 2008, , . | | 1 |
| 20 | WARP, a Unified Wireless Network Testbed for Education and Research. , 2007, , . | | 64 |
| 21 | VLSI Decoder Architecture for High Throughput, Variable Block-size and Multi-rate LDPC Codes. , 2007, , . | | 54 |
| 22 | High Throughput, Parallel, Scalable LDPC Encoder/Decoder Architecture for OFDM Systems. , 2006, , . | | 26 |