Yang Sun

List of Publications by Year
in descending order

22 papers	470 citations	1684188 5 h-index	2053705 5 g-index
23 all docs	23 docs citations	23 times ranked	298 citing authors

#	Article	IF	Citations
1	WARP, a Unified Wireless Network Testbed for Education and Research. , 2007, , .		64
2	VLSI Decoder Architecture for High Throughput, Variable Block-size and Multi-rate LDPC Codes. , 2007, , .		54
3	Implementation of a High Throughput Soft MIMO Detector on GPU. Journal of Signal Processing Systems, 2011, 64, 123-136.	2.1	36
4	Multi-layer parallel decoding algorithm and vlsi architecture for quasi-cyclic LDPC codes. , 2011, , .		31
5	Implementation of a 3GPP LTE turbo decoder accelerator on GPU. , 2010, , .		29
6	A Flexible LDPC/Turbo Decoder Architecture. Journal of Signal Processing Systems, 2011, 64, 1-16.	2.1	27
7	High Throughput, Parallel, Scalable LDPC Encoder/Decoder Architecture for OFDM Systems. , 2006, , .		26
8	A low-power 1-Gbps reconfigurable LDPC decoder design for multiple 4G wireless standards. , 2008, , .		24
9	Trellis-Search Based Soft-Input Soft-Output MIMO Detector: Algorithm and VLSI Architecture. IEEE Transactions on Signal Processing, 2012, 60, 2617-2627.	5.3	24
10	A GPU implementation of a real-time MIMO detector. , 2009, , .		23
11	VLSI Architecture for Layered Decoding of QC-LDPC Codes With High Circulant Weight. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1960-1964.	3.1	22
12	High-Throughput Soft-Output MIMO Detector Based on Path-Preserving Trellis-Search Algorithm. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1235-1247.	3.1	18
13	Reconfigurable real-time MIMO detector on GPU. , 2009, , .		16
14	Scalable and low power LDPC decoder design using high level algorithmic synthesis. , 2009, , .		15
15	GPU accelerated scalable parallel decoding of LDPC codes. , 2011, , .		15
16	Parallel nonbinary LDPC decoding on GPU. , 2012, , .		13
17	Unified decoder architecture for LDPC/turbo codes. , 2008, , .		11
18	FPGA prototyping of a high data rate LTE uplink baseband receiver. , 2009, , .		10

#	Article	IF	Citations
19	High-throughput Contention-Free concurrent interleaver architecture for multi-standard turbo decoder. , 2011, , .		7
20	Low-complexity and high-performance soft MIMO detection based on distributed M-algorithm through trellis-diagram. , 2010, , .		4
21	A new MIMO detector architecture based on a Forward-Backward trellis algorithm. , 2008, , .		1
22	Low complexity scalable MIMO sphere detection through antenna detection reordering. Analog Integrated Circuits and Signal Processing, 2012, 73, 463-472.	1.4	0