

# Xiang Gao

## List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/10647353/publications.pdf>

Version: 2024-02-01

16  
papers

849  
citations

1684188

5  
h-index

2053705

5  
g-index

16  
all docs

16  
docs citations

16  
times ranked

617  
citing authors

#	ARTICLE	IF	CITATIONS
1	A 3.3-4.5GHz Fractional-N Sampling PLL with A Merged Constant Slope DTC and Sampling PD in 40nm CMOS. , 2021, , .		5
2	A calibration-free multi-phase sampling Type-II PLL. , 2021, , .		0
3	Sub-Sampling PLL For Millimeter Wave Applications: An Overview. , 2019, , .		2
4	Low Jitter and Low Power PLLi¼ŹTowards The Utopia. , 2019, , .		3
5	9.6 A 2.7-to-4.3GHz, 0.16psrms-jitter, âˆ²246.8dB-FOM, digital fractional-N sampling PLL in 28nm CMOS. , 2016, , .		33
6	Sub-sampling PLL techniques. , 2015, , .		33
7	20.5 A 40nm dual-band 3-stream 802.11a/b/g/n/ac MIMO WLAN SoC with 1.1Gb/s over-the-air throughput. , 2014, , .		11
8	Flip-Flops for Accurate Multiphase Clocking: Transmission Gate Versus Current Mode Logic. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 422-426.	3.0	7
9	Jitter-Power minimization of digital frequency synthesis architectures. , 2011, , .		5
10	Spur-reduction techniques for PLLs using sub-sampling phase detection. , 2010, , .		20
11	Spur Reduction Techniques for Phase-Locked Loops Exploiting A Sub-Sampling Phase Detector. IEEE Journal of Solid-State Circuits, 2010, 45, 1809-1821.	5.4	183
12	Optimized Stage Ratio of Tapered CMOS Inverters for Minimum Power and Mismatch Jitter Product. , 2010, , .		6
13	Jitter Analysis and a Benchmarking Figure-of-Merit for Phase-Locked Loops. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 117-121.	3.0	224
14	A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is Not Multiplied by $N^2$ . IEEE Journal of Solid-State Circuits, 2009, 44, 3253-3263.	5.4	282
15	Polyphase Multipath Circuits for Cognitive Radio and Flexible Multi-phase Clock Generation. Integrated Circuits and Systems, 2009, , 145-168.	0.2	1
16	Advantages of Shift Registers Over DLLs for Flexible Low Jitter Multiphase Clock Generation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 244-248.	3.0	34