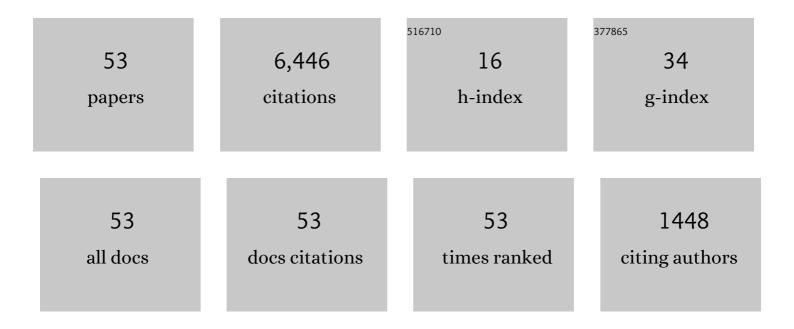
## Anoop Gupta

List of Publications by Year in descending order

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#	Article	IF	CITATIONS
1	Flexible use of memory for replication/migration in cache-coherent DSM multiprocessors. Computer Architecture News, 1998, 26, 342-355.	2.5	6
2	Performance isolation. ACM SIGPLAN Notices, 1998, 33, 181-192.	0.2	7
3	The design and analysis of a cache architecture for texture mapping. Computer Architecture News, 1997, 25, 108-120.	2.5	24
4	Operating system support for improving data locality on CC-NUMA compute servers. Operating Systems Review (ACM), 1996, 30, 279-289.	1.9	14
5	Operating system support for improving data locality on CC-NUMA compute servers. , 1996, , .		176
6	Implementing efficient fault containment for multiprocessors. Communications of the ACM, 1996, 39, 52-61.	4.5	11
7	Operating system support for improving data locality on CC-NUMA compute servers. ACM SIGPLAN Notices, 1996, 31, 279-289.	0.2	22
8	The SPLASH-2 programs. Computer Architecture News, 1995, 23, 24-36.	2.5	458
9	Implications of hierarchical N-body methods for multiprocessor architectures. ACM Transactions on Computer Systems, 1995, 13, 141-202.	0.8	57
10	Memory system performance of UNIX on CC-NUMA multiprocessors. Performance Evaluation Review, 1995, 23, 1-13.	0.6	10
11	The SPLASH-2 programs. , 1995, , .		1,944
12	Integration of message passing and shared memory in the Stanford FLASH multiprocessor. Operating Systems Review (ACM), 1994, 28, 38-50.	1.9	9
13	Scheduling and page migration for multiprocessor compute servers. , 1994, , .		97
14	Interleaving. , 1994, , .		68
15	Performance evaluation of hybrid hardware and software distributed shared memory protocols. , 1994, , .		19
16	The performance impact of flexibility in the Stanford FLASH multiprocessor. , 1994, , .		80
17	Interleaving. Operating Systems Review (ACM), 1994, 28, 308-318.	1.9	6
18	The performance impact of flexibility in the Stanford FLASH multiprocessor. ACM SIGPLAN Notices, 1994, 29, 274-285.	0.2	50

ANOOP GUPTA

#	Article	IF	CITATIONS
19	The performance impact of flexibility in the Stanford FLASH multiprocessor. Operating Systems Review (ACM), 1994, 28, 274-285.	1.9	0
20	Scheduling and page migration for multiprocessor compute servers. ACM SIGPLAN Notices, 1994, 29, 12-24.	0.2	29
21	Integration of message passing and shared memory in the Stanford FLASH multiprocessor. ACM SIGPLAN Notices, 1994, 29, 38-50.	0.2	66
22	Interleaving. ACM SIGPLAN Notices, 1994, 29, 308-318.	0.2	1
23	Scheduling and page migration for multiprocessor compute servers. Operating Systems Review (ACM), 1994, 28, 12-24.	1.9	4
24	Architectural and Implementation Tradeoffs in the Design of Multiple-Context Processors. Kluwer International Series in Engineering and Computer Science, 1994, , 167-200.	0.2	7
25	Working sets, cache sizes, and node granularity issues for large-scale multiprocessors. , 1993, , .		75
26	Data locality and load balancing in COOL. ACM SIGPLAN Notices, 1993, 28, 249-259.	0.2	4
27	Effectiveness of trace sampling for performance debugging tools. Performance Evaluation Review, 1993, 21, 248-259.	0.6	4
28	The DASH prototype. , 1992, , .		99
29	Comparative performance evaluation of cache-coherent NUMA and COMA architectures. , 1992, , .		93
30	SPLASH. Computer Architecture News, 1992, 20, 5-44.	2.5	669
31	Hiding memory latency using dynamic scheduling in shared-memory multiprocessors. , 1992, , .		33
32	The DASH prototype. Computer Architecture News, 1992, 20, 92-103.	2.5	6
33	MemSpy: analyzing memory system bottlenecks in programs. , 1992, , .		86
34	MemSpy: analyzing memory system bottlenecks in programs. Performance Evaluation Review, 1992, 20, 1-12.	0.6	42
35	Design and evaluation of a compiler algorithm for prefetching. ACM SIGPLAN Notices, 1992, 27, 62-73.	0.2	35

Design and evaluation of a compiler algorithm for prefetching. , 1992, , .

ANOOP GUPTA

#	Article	IF	CITATIONS
37	Parallel ICCG on a hierarchical memory multiprocessor — Addressing the triangular solve bottleneck. Parallel Computing, 1992, 18, 719-741.	2.1	30
38	Hiding memory latency using dynamic scheduling in shared-memory multiprocessors. Computer Architecture News, 1992, 20, 22-33.	2.5	17
39	Stanford DASH multiprocessor: The hardware and software approach. Lecture Notes in Computer Science, 1992, , 799-805.	1.3	0
40	Tolerating latency through software-controlled prefetching in shared-memory multiprocessors. Journal of Parallel and Distributed Computing, 1991, 12, 87-106.	4.1	232
41	Comparative evaluation of latency reducing and tolerating techniques. , 1991, , .		110
42	Performance evaluation of memory consistency models for shared-memory multiprocessors. ACM SIGPLAN Notices, 1991, 26, 245-257.	0.2	5
43	Comparative evaluation of latency reducing and tolerating techniques. Computer Architecture News, 1991, 19, 254-263.	2.5	23
44	Performance evaluation of memory consistency models for shared-memory multiprocessors. , 1991, , .		157
45	The impact of operating system scheduling policies and synchronization methods of performance of parallel applications. , 1991, , .		140
46	The directory-based cache coherence protocol for the DASH multiprocessor. Computer Architecture News, 1990, 18, 148-159.	2.5	273
47	Memory consistency and event ordering in scalable shared-memory multiprocessors. , 1990, , .		239
48	Memory consistency and event ordering in scalable shared-memory multiprocessors. Computer Architecture News, 1990, 18, 15-26.	2.5	185
49	The directory-based cache coherence protocol for the DASH multiprocessor. , 1990, , .		147
50	Static and run-time characteristics of OPS5 production systems. Journal of Parallel and Distributed Computing, 1989, 7, 64-95.	4.1	8
51	Parallel implementation of OPS5 on the encore multiprocessor: Results and analysis. International Journal of Parallel Programming, 1988, 17, 95-124.	1.5	34
52	Exploiting variable grain parallelism at runtime. ACM SIGPLAN Notices, 1988, 23, 212-221.	0.2	1
53	Soar/PSM-E: investigating match parallelism in a learning production sytsem. ACM SIGPLAN Notices, 1988, 23, 146-160.	0.2	5