Kartik Mohanram

List of Publications by Year
in descending order

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		567281	752698
52	1,280	15	20
papers	citations	h-index	g-index

52	52	52	1283
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Triple-Mode Single-Transistor Graphene Amplifier and Its Applications. ACS Nano, 2010, 4, 5532-5538.	14.6	168
2	Reliability Analysis of Logic Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 392-405.	2.7	82
3	An Efficient Gate Library for Ambipolar CNTFET Logic. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 242-255.	2.7	78
4	Dual-V_{th} Independent-Gate FinFETs for Low Power Logic Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 337-349.	2.7	69
5	Computational model of edge effects in graphene nanoribbon transistors. Nano Research, 2008, 1, 395-402.	10.4	60
6	TIMBER: Time borrowing and error relaying for online timing error resilience. , 2010, , .		52
7	Graphene Ambipolar Multiplier Phase Detector. IEEE Electron Device Letters, 2011, 32, 1328-1330.	3.9	52
8	Graphene Nanoribbon FETs: Technology Exploration for Performance and Reliability. IEEE Nanotechnology Magazine, 2011, 10, 727-736.	2.0	45
9	SECRET. , 2016, , .		45
10	Modeling stochasticity and robustness in gene regulatory networks. Bioinformatics, 2009, 25, i101-i109.	4.1	43
11	Novel library of logic gates with ambipolar CNTFETs: Opportunities for multi-level logic synthesis. , 2009, , .		40
12	Reliable Nonvolatile Memories: Techniques and Measures. IEEE Design and Test, 2017, 34, 31-41.	1.2	37
13	Time-Borrowing Circuit Designs and Hardware Prototyping for Timing Error Resilience. IEEE Transactions on Computers, 2014, 63, 497-509.	3.4	36
14	Parameter-Variation-Aware Analysis for Noise Robustness. , 2007, , .		34
15	Accurate and scalable reliability analysis of logic circuits. , 2007, , .		34
16	Analytical model for TDDB-based performance degradation in combinational logic. , 2010, , .		30
17	Low Cost Concurrent Error Masking Using Approximate Logic Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1163-1176.	2.7	30
18	CompEx++. Transactions on Architecture and Code Optimization, 2017, 14, 1-30.	2.0	25

#	Article	IF	Citations
19	A model-based technique for efficient evaluation of noise robustness. Midwest Symposium on Circuits and Systems, 2007, , .	1.0	24
20	Analytical model-based technique for efficient evaluation of noise robustness considering parameter variations. Analog Integrated Circuits and Signal Processing, 2009, 60, 27-34.	1.4	24
21	Tunable Transient Filters for Soft Error Rate Reduction in Combinational Circuits. , 2008, , .		23
22	ASSURE. , 2017, , .		23
23	Soft Error Rate Reduction Using Circuit Optimization and Transient Filter Insertion. Journal of Electronic Testing: Theory and Applications (JETTA), 2009, 25, 197-207.	1.2	19
24	Approximate logic circuits for low overhead, non-intrusive concurrent error detection. , 2008, , .		17
25	Modeling and Performance Investigation of the Double-Gate Carbon Nanotube Transistor. IEEE Electron Device Letters, 2011, 32, 231-233.	3.9	16
26	Analytical Theory of Graphene Nanoribbon Transistors. , 2008, , .		14
27	Unequal-error-protection codes in SRAMs for mobile multimedia applications. , 2011, , .		13
28	Design optimization for single-event upset robustness using simultaneous dual-VDD and sizing techniques. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	12
29	Robust 6T Si tunneling transistor SRAM design. , 2011, , .		12
30	Efficient computation of minimal perturbation sets in gene regulatory networks. Frontiers in Physiology, 2013, 4, 361.	2.8	12
31	Masking timing errors on speed-paths in logic circuits. , 2009, , .		11
32	Parallel domain decomposition for simulation of large-scale power grids. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	10
33	High performance reliable variable latency carry select addition. , 2012, , .		10
34	Bi-decomposition of large Boolean functions using blocking edge graphs. , 2010, , .		9
35	Novel dual-V<inf>th</inf> independent-gate FinFET circuits. , 2010, , .		9
36	MFNW: A Flip-N-Write architecture for multi-level cell non-volatile memories. , 2015, , .		9

#	Article	IF	Citations
37	COVERT: Counter OVErflow ReducTion for efficient encryption of non-volatlle memories. , 2017, , .		9
38	ARSENAL: Architecture for Secure Non-Volatile Memories. IEEE Computer Architecture Letters, 2018, 17, 192-196.	1.5	9
39	Compression architecture for bit-write reduction in non-volatile memory technologies. , 2014, , .		7
40	Power consumption of logic circuits in ambipolar carbon nanotube technology. , 2010, , .		6
41	Static window addition: A new paradigm for the design of variable latency adders. , 2011, , .		6
42	ACME: Advanced Counter Mode Encryption for Secure Non-Volatile Memories. , 2018, , .		5
43	Graphene nanoribbon FETs: Technology exploration and CAD. , 2008, , .		3
44	Graphene Transistors and Circuits. , 2011, , 349-376.		3
45	E3R: Energy Efficient Error Recovery for Multi/Triple-Level Cell Non-volatile Memories. , 2016, , .		3
46	L3EP: Low latency, low energy program-and-verify for triple-level cell phase change memory. , 2017, , .		1
47	STASH: SecuriTy Architecture for Smart Hybrid Memories. , 2018, , .		1
48	Ambipolar circuits for analog, mixed-signal, and radio-frequency applications. , 2012, , .		0
49	Mempack: An Order of Magnitude Reduction in the Cost, Risk, and Time for Memory Compiler Certification. , 2013, , .		0
50	Two-Port PCM Architecture for Network Processing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2135-2148.	3.1	0
51	Virtual Two-Port Memory Architecture for Asymmetric Memory Technologies. , 2017, , .		0
52	ASSET: Architectures for Smart Security of Non-Volatile Memories. , 2019, , .		0