Nader Bagherzadeh

List of Publications by Year in Descending Order

187 papers	1,626 citations	20 h-index	29 g-index
206 ext. papers	2,136 ext. citations	2.3 avg, IF	5.23 L-index

#	Paper	IF	Citations
187	A storage-efficient ensemble classification using filter sharing on binarized convolutional neural networks.. *PeerJ Computer Science*, **2022**, 8, e924	2.7	
186	Energy efficient hybrid full adder design for digital signal processing in nanoelectronics. *Analog Integrated Circuits and Signal Processing*, **2021**, 109, 135-151	1.2	0
185	A combined three and five inputs majority gate-based high performance coplanar full adder in quantum-dot cellular automata. *International Journal of Information Technology (Singapore)*, **2021**, 13, 1165-1177	1.4	6
184	Predicting hypotension in the ICU using noninvasive physiological signals. *Computers in Biology and Medicine*, **2021**, 129, 104120	7	3
183	The Effects of Approximate Multiplication on Convolutional Neural Networks. *IEEE Transactions on Emerging Topics in Computing*, **2021**, 1-1	4.1	15
182	Supervised Machine-Learning Algorithms in Real-time Prediction of Hypotensive Events. *Annual International Conference of the IEEE Engineering in Medicine and Biology Society IEEE Engineering in Medicine and Biology Society Annual International Conference*, **2020**, 2020, 5468-5471	0.9	1
181	A high-performance fully programmable membership function generator based on 10□hm gate-all-around CNTFETs. *AEU - International Journal of Electronics and Communications*, **2020**, 123, 153293	2.8	8
180	Reliable and Energy Efficient MLC STT-RAM Buffer for CNN Accelerators. *Computers and Electrical Engineering*, **2020**, 86, 106698	4.3	5
179	Immunity of nanoscale magnetic tunnel junctions with perpendicular magnetic anisotropy to ionizing radiation. *Scientific Reports*, **2020**, 10, 10220	4.9	7
178	IRHT: An SDC detection and recovery architecture based on value locality of instruction binary codes. *Microprocessors and Microsystems*, **2020**, 77, 103159	2.4	2
177	A High Performance, Multi-Bit Output Logic-in-Memory Adder. *IEEE Transactions on Emerging Topics in Computing*, **2020**, 1-1	4.1	1
176	Effect of magnesium oxide adhesion layer on resonance behavior of plasmonic nanostructures. *Applied Physics Letters*, **2020**, 116, 241601	3.4	3
175	A machine-learning approach to predicting hypotensive events in ICU settings. *Computers in Biology and Medicine*, **2020**, 118, 103626	7	10
174	Thermal TSV Optimization and Hierarchical Floorplanning for 3-D Integrated Circuits. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2020**, 10, 599-610	1.7	12
173	. *IEEE Access*, **2020**, 8, 33101-33112	3.5	0
172	Enhancing Reliability of Emerging MemoryTechnology for Machine Learning Accelerators. *IEEE Transactions on Emerging Topics in Computing*, **2020**, 1-1	4.1	3
171	Partition Pruning: Parallelization-Aware Pruning for Dense Neural Networks **2020**,		2

170	Adaptive HTF-MPR. *ACM Transactions on Intelligent Systems and Technology*, **2020**, 11, 1-25	8	9
169	Flow mapping on mesh-based deep learning accelerator. *Journal of Parallel and Distributed Computing*, **2020**, 144, 80-97	4.4	7
168	Divisible load scheduling of image processing applications on the heterogeneous star and tree networks using a new genetic algorithm. *Concurrency Computation Practice and Experience*, **2020**, 32, e5498	1.4	0
167	A novel digital fuzzy system for image edge detection based on wrap-gate carbon nanotube transistors. *Computers and Electrical Engineering*, **2020**, 87, 106811	4.3	4
166	A new approach to the Population-Based Incremental Learning algorithm using virtual regions for task mapping on NoCs. *Journal of Systems Architecture*, **2019**, 97, 443-454	5.5	2
165	A stream-sensitive distributed approach for configuring cascaded classifier topologies in real-time large-scale stream mining systems. *SN Applied Sciences*, **2019**, 1, 1	1.8	1
164	Toward efficient implementation of basic balanced ternary arithmetic operations in CNFET technology. *Microelectronics Journal*, **2019**, 90, 267-277	1.8	4
163	A Radiation Hard Sense Circuit for Spin Transfer Torque Random Access Memory **2019**,		1
162	Catalina: In-Storage Processing Acceleration for Scalable Big Data Analytics **2019**,		6
161	DICA: destination intensity and congestion-aware output selection strategy for network-on-chip systems. *IET Computers and Digital Techniques*, **2019**, 13, 335-347	0.9	4
160	**2019**,		1
159	CLBM: Controlled load-balancing mechanism for congestion management in silicon interposer NoC architecture. *Journal of Systems Architecture*, **2019**, 98, 102-113	5.5	2
158	A Cost-Efficient Iterative Truncated Logarithmic Multiplication for Convolutional Neural Networks **2019**,		10
157	Flow mapping and data distribution on mesh-based deep learning accelerator **2019**,		6
156	Array of symmetric nanohole dimers with high sensitivity for detection of changes in an STT-RAM ultrathin dielectric layer. *Journal of the Optical Society of America B: Optical Physics*, **2019**, 36, 3090	1.7	1
155	Array of Symmetric Nanohole Dimers for STT-RAM Ultrathin Layer Sensing **2019**,		2
154	**2019**,		2
153	Computational storage: an efficient and scalable platform for big data and HPC applications. *Journal of Big Data*, **2019**, 6,	11.7	4

152	Robust Coplanar Full Adder Based on Novel Inverter in Quantum Cellular Automata. *International Journal of Theoretical Physics*, **2019**, 58, 639-655	1.1	10
151	Efficient Mitchell's Approximate Log Multipliers for Convolutional Neural Networks. *IEEE Transactions on Computers*, **2019**, 68, 660-675	2.5	32
150	Novel CNFET ternary circuit techniques for high-performance and energy-efficient design. *IET Circuits, Devices and Systems*, **2019**, 13, 193-202	1.1	17
149	Design and Evaluation of a Spintronic In-Memory Processing Platform for Nonvolatile Data Encryption. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 1788-1801	2.5	26
148	Low-power implementation of Mitchell's approximate logarithmic multiplication for convolutional neural networks **2018**,		6
147	First-Last: A Cost-Effective Adaptive Routing Solution for TSV-Based Three-Dimensional Networks-on-Chip. *IEEE Transactions on Computers*, **2018**, 67, 1430-1444	2.5	12
146	Hospital enterprise Architecture Framework (Study of Iranian University Hospital Organization). *International Journal of Medical Informatics*, **2018**, 114, 88-100	5.3	19
145	LEAD: An Adaptive 3D-NoC Routing Algorithm with Queuing-Theory Based Analytical Verification. *IEEE Transactions on Computers*, **2018**, 1-1	2.5	5
144	A Compositional Approach for Verifying Protocols Running on On-Chip Networks. *IEEE Transactions on Computers*, **2018**, 67, 905-919	2.5	
143	Reducing bypass-based network-on-chip latency using priority mechanism. *IET Computers and Digital Techniques*, **2018**, 12, 1-8	0.9	3
142	HTF-MPR: A heterogeneous TensorFlow mapper targeting performance using genetic algorithms and gradient boosting regressors **2018**,		4
141	Ultra-Efficient Fuzzy Min/Max Circuits Based on Carbon Nanotube FETs. *IEEE Transactions on Fuzzy Systems*, **2018**, 26, 1073-1078	8.3	23
140	STABLE: Stress-Aware Boolean Matching to Mitigate BTI-Induced SNM Reduction in SRAM-Based FPGAs. *IEEE Transactions on Computers*, **2018**, 67, 102-114	2.5	6
139	An energy and area efficient 4:2 compressor based on FinFETs. *The Integration VLSI Journal*, **2018**, 60, 224-231	1.4	22
138	Energy and performance-aware application mapping for inhomogeneous 3D networks-on-chip. *Journal of Systems Architecture*, **2018**, 89, 103-117	5.5	14
137	CompStor: An In-storage Computation Platform for Scalable Distributed Processing **2018**,		7
136	Divisible Load Scheduling of Image Processing Applications on the Heterogeneous Star Network Using a new Genetic Algorithm **2018**,		8
135	Design and Power Analysis of New Coplanar One-Bit Full-Adder Cell in Quantum-Dot Cellular Automata. *Journal of Low Power Electronics*, **2018**, 14, 38-48	1.2	6

134	AROMa: Aging-Aware Deadlock-Free Adaptive Routing Algorithm and Online Monitoring in 3D NoCs. *IEEE Transactions on Parallel and Distributed Systems*, **2018**, 29, 772-788	3.7	4
133	System-Level Analysis of 3D ICs with Thermal TSVs. *ACM Journal on Emerging Technologies in Computing Systems*, **2018**, 14, 1-16	1.7	5
132	Application partitioning and mapping for bypass channel based NoC. *Computers and Electrical Engineering*, **2018**, 71, 676-691	4.3	2
131	A General Fault-Tolerant Minimal Routing for Mesh Architectures. *IEEE Transactions on Computers*, **2017**, 66, 1240-1246	2.5	12
130	A novel low power Exclusive-OR via cell level-based design function in quantum cellular automata. *Journal of Computational Electronics*, **2017**, 16, 875-882	1.8	14
129	Online monitoring and adaptive routing for aging mitigation in NoCs **2017**,		2
128	High-performance ternary operators for scrambling. *The Integration VLSI Journal*, **2017**, 59, 1-9	1.4	3
127	Quantum-dot cellular automata circuits with reduced external fixed inputs. *Microprocessors and Microsystems*, **2017**, 50, 154-163	2.4	33
126	An energy and cost efficient majority-based RAM cell in quantum-dot cellular automata. *Results in Physics*, **2017**, 7, 3543-3551	3.7	30
125	SENSIBle: A Highly Scalable SENsor DeSIgn for Path-Based Age Monitoring in FPGAs. *IEEE Transactions on Computers*, **2017**, 66, 919-926	2.5	14
124	A new approach for designing compressors with a new hardware-friendly mathematical method for multi-input XOR gates. *IET Circuits, Devices and Systems*, **2017**, 11, 46-57	1.1	4
123	Method for designing ternary adder cells based on CNFETs. *IET Circuits, Devices and Systems*, **2017**, 11, 465-470	1.1	23
122	Towards Approximate Computing with Quantum-Dot Cellular Automata. *Journal of Low Power Electronics*, **2017**, 13, 29-35	1.2	4
121	Plasmonic detection of possible defects in multilayer nanohole array consisting of essential materials in simplified STT-RAM cell **2017**,		1
120	On the design of fully symmetrical bridge-style circuits. *IETE Journal of Research*, **2016**, 62, 394-401	0.9	
119	Deadlock Verification of Cache Coherence Protocols and Communication Fabrics. *IEEE Transactions on Computers*, **2016**, 1-1	2.5	3
118	Discontinuous unilateral involvement of 12 part core biopsies by adenocarcinoma predicts bilateral involvement of subsequent radical prostatectomy. *Pathology International*, **2016**, 66, 438-43	1.8	3
117	Design of quaternary 4□ and 5□ compressors for nanotechnology. *Computers and Electrical Engineering*, **2016**, 56, 64-74	4.3	8

116	CoBRA: Low cost compensation of TSV failures in 3D-NoC **2016**,		3
115	Ternary cyclic redundancy check by a new hardware-friendly ternary operator. *Microelectronics Journal*, **2016**, 54, 126-137	1.8	1
114	Ultra-low-power carbon nanotube FET-based quaternary logic gates. *International Journal of Electronics*, **2016**, 1-14	1.2	4
113	Capacitive and Inductive TSV-to-TSV Resilient Approaches for 3D ICs. *IEEE Transactions on Computers*, **2016**, 65, 693-705	2.5	8
112	Loss-Aware Switch Design and Non-Blocking Detection Algorithm for Intra-Chip Scale Photonic Interconnection Networks. *IEEE Transactions on Computers*, **2016**, 65, 1789-1801	2.5	7
111	Performance and Energy Aware Inhomogeneous 3D Networks-on-Chip Architecture Generation. *IEEE Transactions on Parallel and Distributed Systems*, **2016**, 27, 1756-1769	3.7	18
110	An Efficient Analog-to-Digital Converter Based on Carbon Nanotube FETs. *Journal of Low Power Electronics*, **2016**, 12, 150-157	1.2	4
109	A Resilient Routing Algorithm with Formal Reliability Analysis for Partially Connected 3D-NoCs. *IEEE Transactions on Computers*, **2016**, 65, 3265-3279	2.5	26
108	A 3D universal structure based on molecular-QCA and CNT technologies. *Journal of Molecular Structure*, **2016**, 1119, 86-95	3.4	16
107	Fiber dispersion effects in injection-locked optical OFDM systems. *Optical and Quantum Electronics*, **2015**, 47, 3091-3100	2.4	
106	Quaternary full adder cells based on carbon nanotube FETs. *Journal of Computational Electronics*, **2015**, 14, 762-772	1.8	25
105	Robust and energy-efficient carbon nanotube FET-based MVL gates: A novel design approach. *Microelectronics Journal*, **2015**, 46, 1333-1342	1.8	30
104	Advances in multicore systems architectures. *Journal of Supercomputing*, **2015**, 71, 2783-2786	2.5	2
103	Designing quantum-dot cellular automata counters with energy consumption analysis. *Microprocessors and Microsystems*, **2015**, 39, 512-520	2.4	52
102	An Adaptive, Low Restrictive and Fault Resilient Routing Algorithm for 3D Network-on-Chip **2015**,		4
101	Voltage mirror circuit by carbon nanotube field effect transistors for mirroring dynamic random access memories in multiple-valued logic and fuzzy logic. *IET Circuits, Devices and Systems*, **2015**, 9, 343-352	1.1	7
100	Design and Verification of New n-Bit Quantum-Dot Synchronous Counters Using Majority Function-Based JK Flip-Flops. *Journal of Circuits, Systems and Computers*, **2015**, 24, 1550153	0.9	17
99	Design and analysis of a mesh-based wireless network-on-chip. *Journal of Supercomputing*, **2015**, 71, 2830-2846	2.5	19

98	Using constraint programming for the design of network-on-chip architectures. *Computing (Vienna/New York)*, **2015**, 97, 579-592	2.2	1
97	Capacitive Coupling Mitigation for TSV-based 3D ICs **2015**,		4
96	Analytical Fault Tolerance Assessment and Metrics for TSV-Based 3D Network-on-Chip. *IEEE Transactions on Computers*, **2015**, 64, 3591-3604	2.5	26
95	Analytical Reliability Analysis of 3D NoC under TSV Failure. *ACM Journal on Emerging Technologies in Computing Systems*, **2015**, 11, 1-16	1.7	6
94	Accurate System-level TSV-to-TSV Capacitive Coupling Fault Model for 3D-NoC **2015**,		2
93	On the design of hybrid routing mechanism for mesh-based network-on-chip. *The Integration VLSI Journal*, **2015**, 50, 183-192	1.4	3
92	Coupling Mitigation in 3-D Multiple-Stacked Devices. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 2931-2944	2.6	6
91	An Ultra-High Speed and Low Complexity Quantum-Dot Cellular Automata Full Adder. *Journal of Low Power Electronics*, **2015**, 11, 173-180	1.2	8
90	Ultra-low-power adder stage design for exascale floating point units. *Transactions on Embedded Computing Systems*, **2014**, 13, 1-24	1.8	8
89	Voltage island based heterogeneous NoC design through constraint programming. *Computers and Electrical Engineering*, **2014**, 40, 307-316	4.3	3
88	Design and evaluation of a high throughput QoS-aware and congestion-aware router architecture for Network-on-Chip. *Microprocessors and Microsystems*, **2014**, 38, 304-315	2.4	11
87	High-Efficient Circuits for Ternary Addition. *VLSI Design*, **2014**, 2014, 1-15		11
86	TSV-to-TSV inductive coupling-aware coding scheme for 3D Network-on-Chip **2014**,		7
85	A GALS Router for Asynchronous Network-on-Chip **2014**,		3
84	Novel Robust Single Layer Wire Crossing Approach for Exclusive OR Sum of Products Logic Design with Quantum-Dot Cellular Automata. *Journal of Low Power Electronics*, **2014**, 10, 259-271	1.2	113
83	Fault-Tolerant Optimization for Application-Specific Network-on-Chip Architecture. *Lecture Notes in Electrical Engineering*, **2014**, 363-381	0.2	3
82	Efficient multicast schemes for 3-D Networks-on-Chip. *Journal of Systems Architecture*, **2013**, 59, 693-708	5.5	2
81	Scalable load balancing congestion-aware Network-on-Chip router architecture. *Journal of Computer and System Sciences*, **2013**, 79, 421-439	1	20

80	From UML specifications to mapping and scheduling of tasks into a NoC, with reliability considerations. *Journal of Systems Architecture*, **2013**, 59, 429-440	5.5	10
79	Contention-aware selection strategy for application-specific network-on-chip. *IET Computers and Digital Techniques*, **2013**, 7, 105-114	0.9	2
78	CPNoC: On Using Constraint Programming in Design of Network-on-Chip Architecture **2013**,		3
77	On heterogeneous network-on-chip design based on constraint programming **2013**,		1
76	Fully Reliable Dynamic Routing Logic for a Fault-Tolerant NoC Architecture. *Journal of Integrated Circuits and Systems*, **2013**, 8, 43-53	1	2
75	Parallel low-density parity check decoding on a network-on-chip-based multiprocessor platform. *IET Computers and Digital Techniques*, **2012**, 6, 86	0.9	1
74	Design and Evaluation of a High Throughput QoS-Aware and Congestion-Aware Router Architecture for Network-on-Chip **2012**,		5
73	Design and evaluation of a high throughput robust router for network-on-chip. *IET Computers and Digital Techniques*, **2012**, 6, 173	0.9	8
72	LATEX: New Selection Policy for Adaptive Routing in Application-Specific NoC **2012**,		3
71	Design and Analysis of a Mesh-based Wireless Network-on-Chip **2012**,		8
70	Fractional Derivatives Based Scheme for FDTD Modeling of nth-Order Cole□Cole Dispersive Media. *IEEE Antennas and Wireless Propagation Letters*, **2012**, 11, 281-284	3.8	18
69	A load-balanced congestion-aware wireless network-on-chip design for multi-core platforms. *Microprocessors and Microsystems*, **2012**, 36, 555-570	2.4	15
68	A software pipelining algorithm of streaming applications with low buffer requirements. *Scientia Iranica*, **2012**, 19, 627-634	1.5	
67	A formally verified deadlock-free routing function in a fault-tolerant NoC architecture **2012**,		3
66	High-throughput differentiated service provision router architecture for wireless network-on-chip. *International Journal of High Performance Systems Architecture*, **2012**, 4, 38	0.9	
65	A Wireless Network-on-Chip Design for Multicore Platforms **2011**,		46
64	A scheduling approach for distributed resource architectures with scarce communication resources. *International Journal of High Performance Systems Architecture*, **2011**, 3, 12	0.9	1
63	Load Balancing for Data-Parallel Applications on Network-on-Chip Enabled Multi-processor Platform **2011**,		3

62	Area and power-efficient innovative congestion-aware Network-on-Chip architecture. *Journal of Systems Architecture*, **2011**, 57, 24-38	5.5	19
61	Message Driven Programming with S-Net: Methodology and Performance **2010**,		3
60	A scalable delay insensitive asynchronous NoC with adaptive routing **2010**,		6
59	Area and Power-efficient Innovative Network-on-Chip Architecurte **2010**,		5
58	Congestion-aware Network-on-Chip router architecture **2010**,		15
57	Ray tracing on a networked processor array. *International Journal of Electronics*, **2010**, 97, 1193-1205	1.2	3
56	Parallel processing for block ciphers on a fault tolerant networked processor array. *International Journal of High Performance Systems Architecture*, **2010**, 2, 156	0.9	2
55	Scheduling Techniques for Multi-Core Architectures **2009**,		1
54	A Spectral-based partitioning algorithm for parallel LDPC decoding on a multiprocessor platform **2009**,		2
53	PARALLEL FFT ALGORITHMS ON NETWORK-ON-CHIPS. *Journal of Circuits, Systems and Computers*, **2009**, 18, 255-269	0.9	2
52	PERFORMANCE IMPACT OF TASK-TO-TASK COMMUNICATION PROTOCOL IN NETWORK-ON-CHIP. *Journal of Circuits, Systems and Computers*, **2009**, 18, 283-294	0.9	1
51	A framework for low energy data management in reconfigurable multi-context architectures. *Journal of Systems Architecture*, **2009**, 55, 127-139	5.5	
50	A variable frequency link for a power-aware network-on-chip (NoC). *The Integration VLSI Journal*, **2009**, 42, 479-485	1.4	39
49	Resource management and task partitioning and scheduling on a run-time reconfigurable embedded system. *Computers and Electrical Engineering*, **2009**, 35, 258-285	4.3	6
48	A high level power model for Network-on-Chip (NoC) router. *Computers and Electrical Engineering*, **2009**, 35, 837-845	4.3	19
47	Parallel LDPC Decoding on a Network-on-Chip Based Multiprocessor Platform **2009**,		9
46	SecSens - Security Architecture for Wireless Sensor Networks **2009**,		4
45	Parallel and Pipeline Processing for Block Cipher Algorithms on a Network-on-Chip **2009**,		18

44	Gas-leak localization using distributed ultrasonic sensors **2009**,		6
43	Optimisations for LocSens – an indoor location tracking system using wireless sensors. *International Journal of Sensor Networks*, **2009**, 6, 157	0.8	7
42	Design of simulation and analytical models for a 2D-meshed asymmetric adaptive router. *IET Computers and Digital Techniques*, **2008**, 2, 63	0.9	7
41	Scheduling methodology for conditional execution of kernels onto multicontext reconfigurable architectures. *IET Computers and Digital Techniques*, **2008**, 2, 199	0.9	
40	ON DESIGN AND APPLICATION MAPPING OF A NETWORK-ON-CHIP(NOC) ARCHITECTURE. *Parallel Processing Letters*, **2008**, 18, 239-255	0.3	16
39	LocSens - An Indoor Location Tracking System using Wireless Sensors **2008**,		2
38	Parallel FFT Algorithms on Network-on-Chips **2008**,		20
37	An ASIC design and formal analysis of a novel pipelined and parallel sorting accelerator. *The Integration VLSI Journal*, **2008**, 41, 65-75	1.4	1
36	A Generic Network Interface Architecture for a Networked Processor Array (NePA) **2008**, 247-260		9
35	Efficient Parallel Buffer Structure and Its Management Scheme for a Robust Network-on-Chip (NoC) Architecture. *Communications in Computer and Information Science*, **2008**, 98-105	0.3	7
34	Self-optimized Routing in a Network on-a-Chip. *International Federation for Information Processing*, **2008**, 199-212		5
33	Design of a Feasible On-Chip Interconnection Network for a Chip Multiprocessor (CMP) **2007**,		8
32	Application of a Heterogeneous Reconfigurable Architecture to OFDM Wireless Systems **2007**,		2
31	A Modulo Scheduling Algorithm for a Coarse-Grain Reconfigurable Array Template **2007**,		25
30	Ultra-fast and efficient algorithm for energy optimization by gradient-based stochastic voltage and task scheduling. *ACM Transactions on Design Automation of Electronic Systems*, **2007**, 12, 39	1.5	7
29	On Design and Analysis of a Feasible Network-on-Chip (NoC) Architecture **2007**,		18
28	A Study of Implementation of IEEE 802.11 a Physical Layer on a Heterogeneous Reconf1gurable Platform. *International Conference on Advanced Communication Technology*, **2007**,		1
27	Design of a router for network-on-chip. *International Journal of High Performance Systems Architecture*, **2007**, 1, 98	0.9	3

26	A Reconfigurable Processor for Forward Error Correction **2007**, 1-13		1
25	A Coarse-Grain Dynamically Reconfigurable System and Compilation Framework **2007**, 181-215		1
24	A Multi-Standard Viterbi Decoder for Mobile Applications Using a Reconfigurable Architecture **2006**,		6
23	Increasing the throughput of an adaptive router in network-on-chip (NoC) **2006**,		12
22	An efficient voltage scaling algorithm for complex SoCs with few number of voltage modes **2004**,		10
21	Algorithm optimizations and mapping scheme for interactive ray tracing on a reconfigurable architecture. *Computers and Graphics*, **2003**, 27, 701-713	1.8	3
20	A fast parallel reed-solomon decoder on a reconfigurable architecture **2003**,		5
19	IMPACCT: Methodology and Tools for Power-Aware Embedded Systems. *Design Automation for Embedded Systems*, **2002**, 7, 205-232	0.6	3
18	Kernel scheduling techniques for efficient solution space exploration in reconfigurable computing. *Journal of Systems Architecture*, **2001**, 47, 277-292	5.5	6
17	Design and Implementation of the MorphoSys Reconfigurable Computing Processor. *Journal of Signal Processing Systems*, **2000**, 24, 147-164		46
16	MorphoSys **2000**,		32
15	Faster column operations in star networks. *Telecommunication Systems*, **1998**, 10, 33-44	2.3	
14	A scalable register file architecture for superscalar processors. *Microprocessors and Microsystems*, **1998**, 22, 49-60	2.4	
13	Some topological properties of star connected cycles. *Information Processing Letters*, **1996**, 58, 81-85	0.8	
12	A grid embedding into the star graph for image analysis solutions. *Information Processing Letters*, **1996**, 60, 255-260	0.8	4
11	Performance issues of a superscalar microprocessor. *Microprocessors and Microsystems*, **1995**, 19, 187-192	2.4	6
10	Architectural design and analysis of a VLIW processor. *Computers and Electrical Engineering*, **1995**, 21, 119-142	4.3	3
9	A performance comparison of several superscalar processor models with a VLIW processor. *Microprocessors and Microsystems*, **1994**, 18, 131-139	2.4	2

8	The Star Connected Cycles: A Fixed-Degree Network For Parallel Processing **1993**,		9
7	Image processing applications in C++ on a hypercube multicomputer. *Computers and Electrical Engineering*, **1993**, 19, 351-364	4.3	
6	Performance analysis and design methodology for a scalable superscalar architecture. *ACM SIGMICRO Newsletter*, **1992**, 23, 246-255		1
5	Design and implementation of the Tiny RISC microprocessor. *Microprocessors and Microsystems*, **1992**, 16, 187-193	2.4	16
4	Finding circular shapes in an image on a pyramid architecture. *Pattern Recognition Letters*, **1992**, 13, 843-848	4.4	4
3	Near-optimal message routing and broadcasting in faulty hypercubes. *International Journal of Parallel Programming*, **1990**, 19, 405-423	1.5	7
2	Performance of symbolic applications on a parallel architecture. *International Journal of Parallel Programming*, **1987**, 16, 183-214	1.5	3
1	Data scheduling and placement in deep learning accelerator. *Cluster Computing*,1	2.1	2