

Nader Bagherzadeh

List of Publications by Year in descending order

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200
papers

2,615
citations

236912

25
h-index

345203

36
g-index

206
all docs

206
docs citations

206
times ranked

1483
citing authors

#	ARTICLE	IF	CITATIONS
1	Novel Robust Single Layer Wire Crossing Approach for Exclusive OR Sum of Products Logic Design with Quantum-Dot Cellular Automata. Journal of Low Power Electronics, 2014, 10, 259-271.	0.6	148
2	Design and Implementation of the MorphoSys Reconfigurable Computing Processor. Journal of Signal Processing Systems, 2000, 24, 147-164.	1.0	82
3	Efficient Mitchell's Approximate Log Multipliers for Convolutional Neural Networks. IEEE Transactions on Computers, 2019, 68, 660-675.	3.4	74
4	A Wireless Network-on-Chip Design for Multicore Platforms. , 2011, , .		65
5	Designing quantum-dot cellular automata counters with energy consumption analysis. Microprocessors and Microsystems, 2015, 39, 512-520.	2.8	65
6	MorphoSys. , 2000, , .		59
7	An energy and cost efficient majority-based RAM cell in quantum-dot cellular automata. Results in Physics, 2017, 7, 3543-3551.	4.1	49
8	A variable frequency link for a power-aware network-on-chip (NoC). The Integration VLSI Journal, 2009, 42, 479-485.	2.1	46
9	Quantum-dot cellular automata circuits with reduced external fixed inputs. Microprocessors and Microsystems, 2017, 50, 154-163.	2.8	44
10	Analytical Fault Tolerance Assessment and Metrics for TSV-Based 3D Network-on-Chip. IEEE Transactions on Computers, 2015, 64, 3591-3604.	3.4	43
11	A Resilient Routing Algorithm with Formal Reliability Analysis for Partially Connected 3D-NoCs. IEEE Transactions on Computers, 2016, 65, 3265-3279.	3.4	42
12	An energy and area efficient 4:2 compressor based on FinFETs. The Integration VLSI Journal, 2018, 60, 224-231.	2.1	42
13	Robust and energy-efficient carbon nanotube FET-based MVL gates: A novel design approach. Microelectronics Journal, 2015, 46, 1333-1342.	2.0	40
14	Adaptive HTF-MPR. ACM Transactions on Intelligent Systems and Technology, 2020, 11, 1-25.	4.5	38
15	Thermal TSV Optimization and Hierarchical Floorplanning for 3-D Integrated Circuits. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 599-610.	2.5	37
16	Novel CNFET ternary circuit techniques for high performance and energy efficient design. IET Circuits, Devices and Systems, 2019, 13, 193-202.	1.4	35
17	A Modulo Scheduling Algorithm for a Coarse-Grain Reconfigurable Array Template. , 2007, , .		34
18	Parallel FFT Algorithms on Network-on-Chips. , 2008, , .		34

#	ARTICLE	IF	CITATIONS
19	Design and Evaluation of a Spintronic In-Memory Processing Platform for Nonvolatile Data Encryption. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1788-1801.	2.7	34
20	Method for designing ternary adder cells based on CNFETs. IET Circuits, Devices and Systems, 2017, 11, 465-470.	1.4	32
21	Hospital enterprise Architecture Framework (Study of Iranian University Hospital Organization). International Journal of Medical Informatics, 2018, 114, 88-100.	3.3	31
22	The Effects of Approximate Multiplication on Convolutional Neural Networks. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 904-916.	4.6	31
23	On Design and Analysis of a Feasible Network-on-Chip (NoC) Architecture. , 2007, , .		30
24	Area and power-efficient innovative congestion-aware Network-on-Chip architecture. Journal of Systems Architecture, 2011, 57, 24-38.	4.3	30
25	Quaternary full adder cells based on carbon nanotube FETs. Journal of Computational Electronics, 2015, 14, 762-772.	2.5	29
26	A high level power model for Network-on-Chip (NoC) router. Computers and Electrical Engineering, 2009, 35, 837-845.	4.8	28
27	Performance and Energy Aware Inhomogeneous 3D Networks-on-Chip Architecture Generation. IEEE Transactions on Parallel and Distributed Systems, 2016, 27, 1756-1769.	5.6	28
28	Scalable load balancing congestion-aware Network-on-Chip router architecture. Journal of Computer and System Sciences, 2013, 79, 421-439.	1.2	27
29	Ultra-Efficient Fuzzy Min/Max Circuits Based on Carbon Nanotube FETs. IEEE Transactions on Fuzzy Systems, 2018, 26, 1073-1078.	9.8	27
30	Catalina: In-Storage Processing Acceleration for Scalable Big Data Analytics. , 2019, , .		27
31	Design and analysis of a mesh-based wireless network-on-chip. Journal of Supercomputing, 2015, 71, 2830-2846.	3.6	25
32	Design and Verification of New n-Bit Quantum-Dot Synchronous Counters Using Majority Function-Based JK Flip-Flops. Journal of Circuits, Systems and Computers, 2015, 24, 1550153.	1.5	24
33	The Star Connected Cycles: A Fixed-Degree Network For Parallel Processing. , 1993, , .		23
34	Parallel and Pipeline Processing for Block Cipher Algorithms on a Network-on-Chip. , 2009, , .		23
35	A novel low power Exclusive-OR via cell level-based design function in quantum cellular automata. Journal of Computational Electronics, 2017, 16, 875-882.	2.5	23
36	A machine-learning approach to predicting hypotensive events in ICU settings. Computers in Biology and Medicine, 2020, 118, 103626.	7.0	23

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37	Congestion-aware Network-on-Chip router architecture. , 2010, , .		22
38	Fractional Derivatives Based Scheme for FDTD Modeling of n^{th} -Order Dispersive Media. IEEE Antennas and Wireless Propagation Letters, 2012, 11, 281-284.	4.0	22
39	High-Efficient Circuits for Ternary Addition. VLSI Design, 2014, 2014, 1-15.	0.5	22
40	First-Last: A Cost-Effective Adaptive Routing Solution for TSV-Based Three-Dimensional Networks-on-Chip. IEEE Transactions on Computers, 2018, 67, 1430-1444.	3.4	22
41	A Cost-Efficient Iterative Truncated Logarithmic Multiplication for Convolutional Neural Networks. , 2019, , .		22
42	Increasing the throughput of an adaptive router in network-on-chip (NoC). , 2006, , .		21
43	A 3D universal structure based on molecular-QCA and CNT technologies. Journal of Molecular Structure, 2016, 1119, 86-95.	3.6	21
44	SENSIBLE: A Highly Scalable SENSOR DeSIGN for Path-Based Age Monitoring in FPGAs. IEEE Transactions on Computers, 2017, 66, 919-926.	3.4	21
45	Computational storage: an efficient and scalable platform for big data and HPC applications. Journal of Big Data, 2019, 6, .	11.0	20
46	ON DESIGN AND APPLICATION MAPPING OF A NETWORK-ON-CHIP(NOC) ARCHITECTURE. Parallel Processing Letters, 2008, 18, 239-255.	0.6	19
47	A General Fault-Tolerant Minimal Routing for Mesh Architectures. IEEE Transactions on Computers, 2017, 66, 1240-1246.	3.4	19
48	Low-power implementation of Mitchell's approximate logarithmic multiplication for convolutional neural networks. , 2018, , .		19
49	CompStor: An In-storage Computation Platform for Scalable Distributed Processing. , 2018, , .		19
50	Robust Coplanar Full Adder Based on Novel Inverter in Quantum Cellular Automata. International Journal of Theoretical Physics, 2019, 58, 639-655.	1.2	19
51	Immunity of nanoscale magnetic tunnel junctions with perpendicular magnetic anisotropy to ionizing radiation. Scientific Reports, 2020, 10, 10220.	3.3	19
52	Design and implementation of the "Tiny RISC"™ microprocessor. Microprocessors and Microsystems, 1992, 16, 187-193.	2.8	18
53	A load-balanced congestion-aware wireless network-on-chip design for multi-core platforms. Microprocessors and Microsystems, 2012, 36, 555-570.	2.8	18
54	Energy and performance-aware application mapping for inhomogeneous 3D networks-on-chip. Journal of Systems Architecture, 2018, 89, 103-117.	4.3	18

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55	Divisible Load Scheduling of Image Processing Applications on the Heterogeneous Star Network Using a new Genetic Algorithm. , 2018, , .		18
56	SecSens - Security Architecture for Wireless Sensor Networks. , 2009, , .		16
57	An efficient voltage scaling algorithm for complex SoCs with few number of voltage modes. , 2004, , .		15
58	Design and Analysis of a Mesh-based Wireless Network-on-Chip. , 2012, , .		15
59	A combined three and five inputs majority gate-based high performance coplanar full adder in quantum-dot cellular automata. International Journal of Information Technology (Singapore), 2021, 13, 1165-1177.	2.7	14
60	A Generic Network Interface Architecture for a Networked Processor Array (NePA). , 2008, , 247-260.		14
61	Architectural design and analysis of a VLIW processor. Computers and Electrical Engineering, 1995, 21, 119-142.	4.8	13
62	IMPACCT: Methodology and Tools for Power-Aware Embedded Systems. Design Automation for Embedded Systems, 2002, 7, 205-232.	1.0	12
63	From UML specifications to mapping and scheduling of tasks into a NoC, with reliability considerations. Journal of Systems Architecture, 2013, 59, 429-440.	4.3	12
64	Design and evaluation of a high throughput QoS-aware and congestion-aware router architecture for Network-on-Chip. Microprocessors and Microsystems, 2014, 38, 304-315.	2.8	12
65	Design of quaternary 4â€² and 5â€² compressors for nanotechnology. Computers and Electrical Engineering, 2016, 56, 64-74.	4.8	12
66	Capacitive and Inductive TSV-to-TSV Resilient Approaches for 3D ICs. IEEE Transactions on Computers, 2016, 65, 693-705.	3.4	12
67	LEAD: An Adaptive 3D-NoC Routing Algorithm with Queuing-theory Based Analytical Verification. IEEE Transactions on Computers, 2018, , 1-1.	3.4	12
68	A novel digital fuzzy system for image edge detection based on wrap-gate carbon nanotube transistors. Computers and Electrical Engineering, 2020, 87, 106811.	4.8	12
69	Near-optimal message routing and broadcasting in faulty hypercubes. International Journal of Parallel Programming. 1990, 19, 405-423.	1.5	11
70	Ultra-fast and efficient algorithm for energy optimization by gradient-based stochastic voltage and task scheduling. ACM Transactions on Design Automation of Electronic Systems, 2007, 12, 39.	2.6	11
71	A scalable delay insensitive asynchronous NoC with adaptive routing. , 2010, , .		11
72	Design and Evaluation of a High Throughput QoS-Aware and Congestion-Aware Router Architecture for Network-on-Chip. , 2012, , .		11

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73	A high-performance fully programmable membership function generator based on 10Ånm gate-all-around CNTFETs. AEU - International Journal of Electronics and Communications, 2020, 123, 153293.	2.9	11
74	Design and Power Analysis of New Coplanar One-Bit Full-Adder Cell in Quantum-Dot Cellular Automata. Journal of Low Power Electronics, 2018, 14, 38-48.	0.6	11
75	Algorithm optimizations and mapping scheme for interactive ray tracing on a reconfigurable architecture. Computers and Graphics, 2003, 27, 701-713.	2.5	10
76	Design of a Feasible On-Chip Interconnection Network for a Chip Multiprocessor (CMP). , 2007, , .		10
77	A Spectral-based partitioning algorithm for parallel LDPC decoding on a multiprocessor platform. , 2009, , .		10
78	Parallel LDPC Decoding on a Network-on-Chip Based Multiprocessor Platform. , 2009, , .		10
79	Optimisations for LocSens – an indoor location tracking system using wireless sensors. International Journal of Sensor Networks, 2009, 6, 157.	0.4	10
80	Ultra-low-power adder stage design for exascale floating point units. Transactions on Embedded Computing Systems, 2014, 13, 1-24.	2.9	10
81	Gas-leak localization using distributed ultrasonic sensors. Proceedings of SPIE, 2009, , .	0.8	9
82	Loss-Aware Switch Design and Non-Blocking Detection Algorithm for Intra-Chip Scale Photonic Interconnection Networks. IEEE Transactions on Computers, 2016, 65, 1789-1801.	3.4	9
83	STABLE: Stress-Aware Boolean Matching to Mitigate BTI-Induced SNM Reduction in SRAM-Based FPGAs. IEEE Transactions on Computers, 2018, 67, 102-114.	3.4	9
84	System-Level Analysis of 3D ICs with Thermal TSVs. ACM Journal on Emerging Technologies in Computing Systems, 2018, 14, 1-16.	2.3	9
85	Flow mapping and data distribution on mesh-based deep learning accelerator. , 2019, , .		9
86	Toward efficient implementation of basic balanced ternary arithmetic operations in CNFET technology. Microelectronics Journal, 2019, 90, 267-277.	2.0	9
87	Reliable and Energy Efficient MLC STT-RAM Buffer for CNN Accelerators. Computers and Electrical Engineering, 2020, 86, 106698.	4.8	9
88	Flow mapping on mesh-based deep learning accelerator. Journal of Parallel and Distributed Computing, 2020, 144, 80-97.	4.1	9
89	An Ultra-High Speed and Low Complexity Quantum-Dot Cellular Automata Full Adder. Journal of Low Power Electronics, 2015, 11, 173-180.	0.6	9
90	Kernel scheduling techniques for efficient solution space exploration in reconfigurable computing. Journal of Systems Architecture, 2001, 47, 277-292.	4.3	8

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91	A Multi-Standard Viterbi Decoder for Mobile Applications Using a Reconfigurable Architecture. , 2006, , .		8
92	Design of simulation and analytical models for a 2D-meshed asymmetric adaptive router. IET Computers and Digital Techniques, 2008, 2, 63.	1.2	8
93	Area and Power-efficient Innovative Network-on-Chip Architecture. , 2010, , .		8
94	Design and evaluation of a high throughput robust router for network-on-chip. IET Computers and Digital Techniques, 2012, 6, 173.	1.2	8
95	TSV-to-TSV inductive coupling-aware coding scheme for 3D Network-on-Chip. , 2014, , .		8
96	Voltage mirror circuit by carbon nanotube field effect transistors for mirroring dynamic random access memories in multiple-valued logic and fuzzy logic. IET Circuits, Devices and Systems, 2015, 9, 343-352.	1.4	8
97	Ultra-low-power carbon nanotube FET-based quaternary logic gates. International Journal of Electronics, 0, , 1-14.	1.4	8
98	Accelerating HPC Applications Using Computational Storage Devices. , 2019, , .		8
99	Self-optimized Routing in a Network on-a-Chip. International Federation for Information Processing, 2008, , 199-212.	0.4	8
100	Efficient Parallel Buffer Structure and Its Management Scheme for a Robust Network-on-Chip (NoC) Architecture. Communications in Computer and Information Science, 2008, , 98-105.	0.5	8
101	Analytical Reliability Analysis of 3D NoC under TSV Failure. ACM Journal on Emerging Technologies in Computing Systems, 2015, 11, 1-16.	2.3	7
102	DICA: destination intensity and congestion-aware output selection strategy for network-on-chip systems. IET Computers and Digital Techniques, 2019, 13, 335-347.	1.2	7
103	Effect of magnesium oxide adhesion layer on resonance behavior of plasmonic nanostructures. Applied Physics Letters, 2020, 116, .	3.3	7
104	Predicting hypotension in the ICU using noninvasive physiological signals. Computers in Biology and Medicine, 2021, 129, 104120.	7.0	7
105	A fast parallel reed-solomon decoder on a reconfigurable architecture. , 2003, , .		7
106	A performance comparison of several superscalar processor models with a VLIW processor. Microprocessors and Microsystems, 1994, 18, 131-139.	2.8	6
107	Performance issues of a superscalar microprocessor. Microprocessors and Microsystems, 1995, 19, 187-199.	2.8	6
108	Application of a Heterogeneous Reconfigurable Architecture to OFDM Wireless Systems. , 2007, , .		6

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109	Resource management and task partitioning and scheduling on a run-time reconfigurable embedded system. Computers and Electrical Engineering, 2009, 35, 258-285.	4.8	6
110	Voltage island based heterogeneous NoC design through constraint programming. Computers and Electrical Engineering, 2014, 40, 307-316.	4.8	6
111	Coupling Mitigation in 3-D Multiple-Stacked Devices. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2931-2944.	3.1	6
112	CoBRA: Low cost compensation of TSV failures in 3D-NoC. , 2016, , .		6
113	A new approach for designing compressors with a new hardware-friendly mathematical method for multi-input XOR gates. IET Circuits, Devices and Systems, 2017, 11, 46-57.	1.4	6
114	AROMA: Aging-Aware Deadlock-Free Adaptive Routing Algorithm and Online Monitoring in 3D NoCs. IEEE Transactions on Parallel and Distributed Systems, 2018, 29, 772-788.	5.6	6
115	A High Performance, Multi-Bit Output Logic-in-Memory Adder. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 2223-2233.	4.6	6
116	An Efficient Analog-to-Digital Converter Based on Carbon Nanotube FETs. Journal of Low Power Electronics, 2016, 12, 150-157.	0.6	6
117	Towards Approximate Computing with Quantum-Dot Cellular Automata. Journal of Low Power Electronics, 2017, 13, 29-35.	0.6	6
118	Performance of symbolic applications on a parallel architecture. International Journal of Parallel Programming, 1987, 16, 183-214.	1.5	5
119	A grid embedding into the star graph for image analysis solutions. Information Processing Letters, 1996, 60, 255-260.	0.6	5
120	Design of a router for network-on-chip. International Journal of High Performance Systems Architecture, 2007, 1, 98.	0.3	5
121	LocSens - An Indoor Location Tracking System using Wireless Sensors. , 2008, , .		5
122	A GALS Router for Asynchronous Network-on-Chip. , 2014, , .		5
123	An Adaptive, Low Restrictive and Fault Resilient Routing Algorithm for 3D Network-on-Chip. , 2015, , .		5
124	High-performance ternary operators for scrambling. The Integration VLSI Journal, 2017, 59, 1-9.	2.1	5
125	HTF-MPR: A heterogeneous TensorFlow mapper targeting performance using genetic algorithms and gradient boosting regressors. , 2018, , .		5
126	Efficient Deep Neural Networks for Edge Computing. , 2019, , .		5

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127	Enhancing Reliability of Emerging Memory Technology for Machine Learning Accelerators. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 2234-2240.	4.6	5
128	Finding circular shapes in an image on a pyramid architecture. Pattern Recognition Letters, 1992, 13, 843-848.	4.2	4
129	An ASIC design and formal analysis of a novel pipelined and parallel sorting accelerator. The Integration VLSI Journal, 2008, 41, 65-75.	2.1	4
130	Load Balancing for Data-Parallel Applications on Network-on-Chip Enabled Multi-processor Platform. , 2011, , .		4
131	Efficient multicast schemes for 3-D Networks-on-Chip. Journal of Systems Architecture, 2013, 59, 693-708.	4.3	4
132	Capacitive Coupling Mitigation for TSV-based 3D ICs. , 2015, , .		4
133	Deadlock Verification of Cache Coherence Protocols and Communication Fabrics. IEEE Transactions on Computers, 2016, , 1-1.	3.4	4
134	Online monitoring and adaptive routing for aging mitigation in NoCs. , 2017, , .		4
135	Power and Performance Optimal NoC Design for CPU-GPU Architecture Using Formal Models. , 2019, , .		4
136	Divisible load scheduling of image processing applications on the heterogeneous star and tree networks using a new genetic algorithm. Concurrency Computation Practice and Experience, 2020, 32, e5498.	2.2	4
137	Supervised Machine-Learning Algorithms in Real-time Prediction of Hypotensive Events. , 2020, 2020, 5468-5471.		4
138	IRHT: An SDC detection and recovery architecture based on value locality of instruction binary codes. Microprocessors and Microsystems, 2020, 77, 103159.	2.8	4
139	Message Driven Programming with S-Net: Methodology and Performance. , 2010, , .		3
140	Ray tracing on a networked processor array. International Journal of Electronics, 2010, 97, 1193-1205.	1.4	3
141	LATEX: New Selection Policy for Adaptive Routing in Application-Specific NoC. , 2012, , .		3
142	A formally verified deadlock-free routing function in a fault-tolerant NoC architecture. , 2012, , .		3
143	CPNoC: On Using Constraint Programming in Design of Network-on-Chip Architecture. , 2013, , .		3
144	On the design of hybrid routing mechanism for mesh-based network-on-chip. The Integration VLSI Journal, 2015, 50, 183-192.	2.1	3

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145	Using constraint programming for the design of network-on-chip architectures. Computing (Vienna/New York), 2015, 97, 579-592.	4.8	3
146	Discontinuous unilateral involvement of 12 part core biopsies by adenocarcinoma predicts bilateral involvement of subsequent radical prostatectomy. Pathology International, 2016, 66, 438-443.	1.3	3
147	Ternary cyclic redundancy check by a new hardware-friendly ternary operator. Microelectronics Journal, 2016, 54, 126-137.	2.0	3
148	Reducing bypass-based network-on-chip latency using priority mechanism. IET Computers and Digital Techniques, 2018, 12, 1-8.	1.2	3
149	A new approach to the Population-Based Incremental Learning algorithm using virtual regions for task mapping on NoCs. Journal of Systems Architecture, 2019, 97, 443-454.	4.3	3
150	Fault-Tolerant Optimization for Application-Specific Network-on-Chip Architecture. Lecture Notes in Electrical Engineering, 2014, , 363-381.	0.4	3
151	Array of symmetric nanohole dimers with high sensitivity for detection of changes in an STT-RAM ultrathin dielectric layer. Journal of the Optical Society of America B: Optical Physics, 2019, 36, 3090.	2.1	3
152	Fully Reliable Dynamic Routing Logic for a Fault-Tolerant NoC Architecture. Journal of Integrated Circuits and Systems, 2013, 8, 43-53.	0.4	3
153	Performance analysis and design methodology for a scalable superscalar architecture. ACM SIGMICRO Newsletter, 1992, 23, 246-255.	0.4	2
154	A Study of Implementation of IEEE 802.11 a Physical Layer on a Heterogeneous Reconfigurable Platform. International Conference on Advanced Communication Technology, 2007, , .	0.0	2
155	Performance Impact of Task-to-Task Communication Protocol in Network-on-Chip. , 2008, , .		2
156	PARALLEL FFT ALGORITHMS ON NETWORK-ON-CHIPS. Journal of Circuits, Systems and Computers, 2009, 18, 255-269.	1.5	2
157	Parallel processing for block ciphers on a fault tolerant networked processor array. International Journal of High Performance Systems Architecture, 2010, 2, 156.	0.3	2
158	Parallel low-density parity check decoding on a network-on-chip-based multiprocessor platform. IET Computers and Digital Techniques, 2012, 6, 86.	1.2	2
159	Contention-aware selection strategy for application-specific network-on-chip. IET Computers and Digital Techniques, 2013, 7, 105-114.	1.2	2
160	On heterogeneous network-on-chip design based on constraint programming. , 2013, , .		2
161	Accurate System-level TSV-to-TSV Capacitive Coupling Fault Model for 3D-NoC. , 2015, , .		2
162	Advances in multicore systems architectures. Journal of Supercomputing, 2015, 71, 2783-2786.	3.6	2

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163	Application partitioning and mapping for bypass channel based NoC. Computers and Electrical Engineering, 2018, 71, 676-691.	4.8	2
164	CLBM: Controlled load-balancing mechanism for congestion management in silicon interposer NoC architecture. Journal of Systems Architecture, 2019, 98, 102-113.	4.3	2
165	Data scheduling and placement in deep learning accelerator. Cluster Computing, 0, , 1.	5.0	2
166	Array of Symmetric Nanohole Dimers for STT-RAM Ultrathin Layer Sensing. , 2019, , .		2
167	Partition Pruning: Parallelization-Aware Pruning for Dense Neural Networks. , 2020, , .		2
168	Scheduling Techniques for Multi-Core Architectures. , 2009, , .		1
169	Low power adaptive pipeline based on instruction isolation. , 2009, , .		1
170	PERFORMANCE IMPACT OF TASK-TO-TASK COMMUNICATION PROTOCOL IN NETWORK-ON-CHIP. Journal of Circuits, Systems and Computers, 2009, 18, 283-294.	1.5	1
171	A scheduling approach for distributed resource architectures with scarce communication resources. International Journal of High Performance Systems Architecture, 2011, 3, 12.	0.3	1
172	Quality of Service Optimization for Network-on-Chip Using Bandwidth-Constraint Mapping Algorithm. , 2013, , .		1
173	Multicore computing systems: Architecture, programming tools, and applications. Journal of Computer and System Sciences, 2013, 79, 403-405.	1.2	1
174	Special issue on on-chip parallel and network-based systems. Computing (Vienna/New York), 2015, 97, 539-541.	4.8	1
175	Simulation-Based Evaluation Strategy for Task Mapping Approaches in WNoC Platforms. , 2018, , .		1
176	A stream-sensitive distributed approach for configuring cascaded classifier topologies in real-time large-scale stream mining systems. SN Applied Sciences, 2019, 1, 1.	2.9	1
177	A Radiation Hard Sense Circuit for Spin Transfer Torque Random Access Memory. , 2019, , .		1
178	A Fine-Grained Source-Throttling Method for Mesh Architectures. IEEE Access, 2020, 8, 33101-33112.	4.2	1
179	Energy efficient hybrid full adder design for digital signal processing in nanoelectronics. Analog Integrated Circuits and Signal Processing, 2021, 109, 135-151.	1.4	1
180	A Coarse-Grain Dynamically Reconfigurable System and Compilation Framework. , 2007, , 181-215.		1

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181	Plasmonic detection of possible defects in multilayer nanohole array consisting of essential materials in simplified STT-RAM cell. , 2017, , .		1
182	Image processing applications in C++ on a hypercube multicomputer. Computers and Electrical Engineering, 1993, 19, 351-364.	4.8	0
183	Some topological properties of star connected cycles. Information Processing Letters, 1996, 58, 81-85.	0.6	0
184	Faster column operations in star networks. Telecommunication Systems, 1998, 10, 33-44.	2.5	0
185	A scalable register file architecture for superscalar processors. Microprocessors and Microsystems, 1998, 22, 49-60.	2.8	0
186	A Distributed and Shared Register File for a Multiprocessor-on-Chip to Support Real-Time Applications. , 2006, , .		0
187	Integrating Power Management into Distributed Real-time Systems at Very Low Implementation Cost. , 2007, , .		0
188	Scheduling methodology for conditional execution of kernels onto multicontext reconfigurable architectures. IET Computers and Digital Techniques, 2008, 2, 199.	1.2	0
189	A framework for low energy data management in reconfigurable multi-context architectures. Journal of Systems Architecture, 2009, 55, 127-139.	4.3	0
190	Editorial: High-performance computing system architectures: design and performance. IET Computers and Digital Techniques, 2012, 6, 257-258.	1.2	0
191	High-throughput differentiated service provision router architecture for wireless network-on-chip. International Journal of High Performance Systems Architecture, 2012, 4, 38.	0.3	0
192	A software pipelining algorithm of streaming applications with low buffer requirements. Scientia Iranica, 2012, 19, 627-634.	0.4	0
193	Fiber dispersion effects in injection-locked optical OFDM systems. Optical and Quantum Electronics, 2015, 47, 3091-3100.	3.3	0
194	On the design of fully symmetrical bridge-style circuits. IETE Journal of Research, 2016, 62, 394-401.	2.6	0
195	A Compositional Approach for Verifying Protocols Running on On-Chip Networks. IEEE Transactions on Computers, 2018, 67, 905-919.	3.4	0
196	Optoelectronic Readout of STT-RAM Memory Cells Using Plasmon Drag Effect. , 2021, , .		0
197	Effect of Tantalum and MgO adhesion layers on plasmonic nanostructures. , 2019, , .		0
198	Thermal Analysis of 3D ICs With TSVs Placement Optimization. , 2019, , .		0

#	ARTICLE	IF	CITATIONS
199	Guest Editorial: Thematic Section on Applications of Emerging Computing Technologies in Smart Manufacturing and Industry 4.0. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 6-8.	4.6	0
200	A storage-efficient ensemble classification using filter sharing on binarized convolutional neural networks. PeerJ Computer Science, 2022, 8, e924.	4.5	0