Susan J Eggers

List of Publications by Year
in descending order

26 papers	843 citations	1307594 7 h-index	888059 17 g-index
26 all docs	26 docs citations	26 times ranked	235 citing authors

#	Article	IF	Citations
1	Instruction scheduling for a tiled dataflow architecture. Computer Architecture News, 2006, 34, 141-150.	2.5	2
2	Balanced scheduling. ACM SIGPLAN Notices, 2004, 39, 515-527.	0.2	1
3	A retrospective on. ACM SIGPLAN Notices, 2004, 39, 656-669.	0.2	3
4	Towards automatic construction of staged compilers. , 2002, , .		7
5	Towards automatic construction of staged compilers. ACM SIGPLAN Notices, 2002, 37, 113-125.	0.2	2
6	DyC: an expressive annotation-directed dynamic compiler for C. Theoretical Computer Science, 2000, 248, 147-199.	0.9	97
7	Calpa. , 2000, , .		45
8	The benefits and costs of DyC's run-time optimizations. ACM Transactions on Programming Languages and Systems, 2000, 22, 932-972.	2.1	19
9	An evaluation of staged run-time optimizations in DyC. , 1999, , .		95
10	An evaluation of staged run-time optimizations in DyC. ACM SIGPLAN Notices, 1999, 34, 293-304.	0.2	6
11	An analysis of database workload performance on simultaneous multithreaded processors. Computer Architecture News, 1998, 26, 39-50.	2.5	17
12	Annotation-directed run-time specialization in C. , 1997, , .		58
13	Annotation-directed run-time specialization in C. ACM SIGPLAN Notices, 1997, 32, 163-178.	0.2	7
14	Fast, effective dynamic compilation. ACM SIGPLAN Notices, 1996, 31, 149-159.	0.2	20
15	Fast, effective dynamic compilation. , 1996, , .		123
16	Reducing false sharing on shared memory multiprocessors through compile time data transformations. ACM SIGPLAN Notices, 1995, 30, 179-188.	0.2	18
17	Improving balanced scheduling with compiler optimizations that increase instruction-level parallelism. , 1995, , .		16
18	Improving balanced scheduling with compiler optimizations that increase instruction-level parallelism. ACM SIGPLAN Notices, 1995, 30, 151-162.	0.2	6

#	Article	IF	Citations
19	Simultaneous multithreading. Computer Architecture News, 1995, 23, 392-403.	2.5	126
20	The effectiveness of multiple hardware contexts. Operating Systems Review (ACM), 1994, 28, 328-337.	1.9	6
21	The effectiveness of multiple hardware contexts. ACM SIGPLAN Notices, 1994, 29, 328-337.	0.2	7
22	Balanced scheduling. , 1993, , .		37
23	Integrating register allocation and instruction scheduling for RISCs. , 1991, , .		89
24	On the validity of trace-driven simulation for multiprocessors. Computer Architecture News, 1991, 19, 244-253.	2.5	1
25	The effect on RISC performance of register set size and structure versus code generation strategy. Computer Architecture News, 1991, 19, 330-339.	2.5	1
26	The Marion system for retargetable instruction scheduling. , 1991, , .		34