Bruce Jacob

List of Publications by Year
in descending order

25 papers	1,437 citations	1163117 8 h-index	1058476 14 g-index
25 all docs	25 docs citations	25 times ranked	770 citing authors

#	Article	IF	Citations
1	DRAMSim2: A Cycle Accurate Memory System Simulator. IEEE Computer Architecture Letters, 2011, 10, 16-19.	1.5	696
2	DRAMsim. Computer Architecture News, 2005, 33, 100-107.	2.5	257
3	DRAMsim3: A Cycle-Accurate, Thermal-Capable DRAM Simulator. IEEE Computer Architecture Letters, 2020, 19, 106-109.	1.5	87
4	Flexible auto-refresh. , 2015, , .		72
5	Fully-Buffered DIMM Memory Architectures: Understanding Mechanisms, Overheads and Scaling. , 2007, , .		66
6	Concurrency, latency, or system overhead. , 2001, , .		52
7	Fine-Grained Activation for Power Reduction in DRAM. IEEE Micro, 2010, 30, 34-47.	1.8	46
8	The performance of PC solid-state disks (SSDs) as a function of bandwidth, concurrency, device architecture, and system organization. Computer Architecture News, 2009, 37, 279-289.	2.5	39
9	The Memory System: You Can't Avoid It, You Can't Ignore It, You Can't Fake It. Synthesis Lectures on Computer Architecture, 2009, 4, 1-77.	1.3	23
10	A performance & power comparison of modern high-speed DRAM architectures. , 2018, , .		22
11	Coordinated refresh: Energy efficient techniques for DRAM refresh scheduling. , 2013, , .		16
12	Flexible auto-refresh. Computer Architecture News, 2016, 43, 235-246.	2.5	13
13	Electromagnetic Interference and Digital Circuits: An Initial Study of Clock Networks. Electromagnetics, 2006, 26, 73-86.	0.7	9
14	Buffer-on-board memory systems. Computer Architecture News, 2012, 40, 392-403.	2.5	9
15	Main memory latency simulation. , 2018, , .		5
16	Statistical DRAM modeling. , 2019, , .		5
17	The 2 PetaFLOP, 3 Petabyte, 9 TB/s, 90ÂkW Cabinet: A System Architecture for Exascale and Big Data. IEEE Computer Architecture Letters, 2016, 15, 125-128.	1.5	4
18	Rethinking cycle accurate DRAM simulation. , 2019, , .		4

#	Article	IF	Citations
19	Analyzing the Monolithic Integration of a ReRAM-Based Main Memory Into a CPU's Die. IEEE Micro, 2019, 39, 64-72.	1.8	3
20	Monolithically Integrating Non-Volatile Main Memory over the Last-Level Cache. Transactions on Architecture and Code Optimization, 2021, 18, 1-26.	2.0	3
21	The Case for VLIW-CMP as a Building Block for Exascale. IEEE Computer Architecture Letters, 2016, 15, 54-57.	1.5	2
22	PROFET. Proceedings of the ACM on Measurement and Analysis of Computing Systems, 2019, 3, 1-33.	1.8	2
23	Bringing Modern Hierarchical Memory Systems Into Focus. , 2015, , .		1
24	Tileable Monolithic ReRAM Memory Design. , 2020, , .		1
25	An analytical model to estimate PCM failure probability due to process variations. , 2011, , .		0