Syed Rafay Hasan

List of Publications by Year
in descending order

45	304	1163117 8	1125743 13
papers	citations	h-index	g-index

45	45	45	197
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Power profiling of microcontroller's instruction set for runtime hardware Trojans detection without golden circuit models. , 2017, , .		25
2	MulNet: A Flexible CNN Processor With Higher Resource Utilization Efficiency for Constrained Devices. IEEE Access, 2019, 7, 47509-47524.	4.2	20
3	FPGA-Based Convolutional Neural Network Architecture with Reduced Parameter Requirements. , 2018, , .		19
4	Runtime hardware Trojan monitors through modeling burst mode communication using formal verification. The Integration VLSI Journal, 2018, 61, 62-76.	2.1	18
5	Characterizing, modeling, and analyzing soft error propagation in asynchronous and synchronous digital circuits. Microelectronics Reliability, 2015, 55, 238-250.	1.7	17
6	Hardware trojans in 3-D ICs due to NBTI effects and countermeasure. The Integration VLSI Journal, 2017, 59, 64-74.	2.1	16
7	New Insights Into the Single Event Transient Propagation Through Static and TSPC Logic. IEEE Transactions on Nuclear Science, 2014, 61, 1618-1627.	2.0	15
8	Self-triggering hardware trojan: Due to NBTI related aging in 3-D ICs. The Integration VLSI Journal, 2017, 58, 116-124.	2.1	14
9	MacLeR: Machine Learning-Based Runtime Hardware Trojan Detection in Resource-Constrained IoT Edge Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3748-3761.	2.7	12
10	Hardware Trojan detection in soft error tolerant macro synchronous micro asynchronous (MSMA) pipeline. , 2014, , .		10
11	Formal reliability analysis of protective systems in smart grids. , 2016, , .		10
12	Modeling, analyzing, and abstracting single event transient propagation at gate level. , 2014, , .		9
13	Low Power Soft Error Tolerant Macro Synchronous Micro Asynchronous (MSMA) Pipeline. , 2014, , .		9
14	Formal verification of ladder logic programs using NuSMV. , 2017, , .		9
15	Intrusion Detection in PLC-Based Industrial Control Systems Using Formal Verification Approach in Conjunction with Graphs. Journal of Hardware and Systems Security, 2018, 2, 1-14.	1.3	9
16	Crosstalk Glitch Propagation Modeling for Asynchronous Interfaces in Globally Asynchronous Locally Synchronous Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2020-2031.	5.4	8
17	Formal Asymptotic Analysis of Online Scheduling Algorithms for Plug-In Electric Vehiclesâ€™ Charging. Energies, 2019, 12, 19.	3.1	8
18	Analyzing Vulnerability of Asynchronous Pipeline to Soft Errors: Leveraging Formal Verification. Journal of Electronic Testing: Theory and Applications (JETTA), 2016, 32, 569-586.	1.2	6

#	Article	IF	Citations
19	MulMapper: Towards an Automated FPGA-Based CNN Processor Generator Based on a Dynamic Design Space Exploration. , 2019, , .		6
20	SIMCom: Statistical sniffing of inter-module communications for runtime hardware trojan detection. Microprocessors and Microsystems, 2020, 77, 103122.	2.8	6
21	Hardware Trojan Based Security Issues in Home Area Network: A Testbed Setup. , 2018, , .		5
22	Formal Reliability Analysis of an Integrated Power Generation System Using Theorem Proving. IEEE Systems Journal, 2020, 14, 4820-4831.	4.6	5
23	An all-digital skew-adaptive clock scheduling algorithm for heterogeneous multiprocessor systems on chips (MPSoCs). , 2009, , .		4
24	Investigating the impact of propagation paths and re-convergent paths on the propagation induced pulse broadening. , 2013, , .		4
25	Introducing redundant TSV with low inductance for 3-D IC. , 2014, , .		4
26	Covert Communication Channel Detection in Low-Power Battery Operated IoT Devices: Leveraging Power Profiles. , 2018, , .		4
27	Identification of soft error glitch-propagation paths: Leveraging SAT solvers. , 2012, , .		3
28	Timing variation aware dynamic digital phase detector for lowâ€latency clock domain crossing. IET Circuits, Devices and Systems, 2014, 8, 58-64.	1.4	3
29	Abstracting Single Event Transient characteristics variations due to input patterns and fan-out. , 2014, , .		3
30	Area efficient soft error tolerant RISC pipeline: Leveraging data encoding and inherent ALU redundancy. , 2017, , .		3
31	A novel correlation power analysis attack on PIC based AES-128 without access to crypto device. , 2017, , .		3
32	2L-3W: 2-Level 3-Way Hardwareâ€“Software Co-verification for the Mapping of Convolutional Neural Network (CNN) onto FPGA Boards. SN Computer Science, 2022, 3, 1.	3.6	3
33	Split H-tree Design Method for High-Performance GALS Systems. , 2006, , .		2
34	Metastability tolerant mesochronous synchronization. Midwest Symposium on Circuits and Systems, 2007, , .	1.0	2
35	All-digital skew-tolerant interfacing method for systems with rational frequency ratios among Multiple Clock Domains: Leveraging a priori timing information. , 2008, , .		2
36	SEGP-Finder: Tool for identification of Soft Error Glitch-Propagating paths at gate level. , 2011, , .		2

#	Article	IF	Citations
37	Formal verification of demand response based home energy management systems in smart grids. , 2017, , .		2
38	Crosstalk Effects in Event-Driven Self-Timed Circuits Designed With 90nm CMOS Technology. , 2007, , .		1
39	Grouped through silicon vias for lower L d i /d t drop in threeâ€dimensional integrated circuit. IET Circuits, Devices and Systems, 2016, 10, 44-53.	1.4	1
40	Deployment of Object Detection Enhanced with Multi-label Multi-classification on Edge Device. , 2020, , .		1
41	InTrust-IoT: Intelligent Ecosystem based on Power Profiling of Trusted device(s) in IoT for Hardware Trojan Detection. , 2021, , .		1
42	Towards low area overhead ARQ based soft error tolerant data paths for SRAM-based Altera FPGAs. , 2012, , .		0
43	All Digital Low Power Aging Sensor for Counterfeit Detection in Integrated Circuits. , 2018, , .		0
44	Dynamic Distribution of Edge Intelligence at the Node Level for Internet of Things. , 2021, , .		0
45	LaBaNI: Layer-based Noise Injection Attack on Convolutional Neural Networks. , 2022, , .		0