

Xin Lou

List of Publications by Year in descending order

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187
citing authors

#	ARTICLE	IF	CITATIONS
1	Radar-Based Human Activity Recognition With 1-D Dense Attention Network. IEEE Geoscience and Remote Sensing Letters, 2022, 19, 1-5.	1.4	8
2	A Raw Image-Based End-to-End Object Detection Accelerator Using HOG Features. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 322-333.	3.5	11
3	FPGA Accelerator for Real-Time Non-Line-of-Sight Imaging. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 721-734.	3.5	5
4	Reconfigurable Nonuniform Filter Bank for Hearing Aid Systems. IEEE/ACM Transactions on Audio Speech and Language Processing, 2022, 30, 758-771.	4.0	8
5	Multi-Level Time-Frequency Bins Selection for Direction of Arrival Estimation Using a Single Acoustic Vector Sensor. IEEE/ACM Transactions on Audio Speech and Language Processing, 2022, 30, 1048-1060.	4.0	2
6	A Block PatchMatch-Based Energy-Resource Efficient Stereo Matching Processor on FPGA. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2893-2905.	3.5	1
7	Multiplication and Accumulation Co-Optimization for Low Complexity FIR Filter Implementation. Electronics (Switzerland), 2022, 11, 1721.	1.8	0
8	A Time-Frequency Bins Selection Pipeline for Direction-of-Arrival Estimation Using a Single Acoustic Vector Sensor. IEEE Sensors Journal, 2022, 22, 14306-14319.	2.4	1
9	RadarSpecAugment: A Simple Data Augmentation Method for Radar-Based Human Activity Recognition. , 2021, 5, 1-4.		6
10	Multi-Scale Slanted O(1) Stereo Matching Algorithm. , 2021, , .		0
11	Lightweight Deep Learning Model in Mobile-Edge Computing for Radar-Based Human Activity Recognition. IEEE Internet of Things Journal, 2021, 8, 12350-12359.	5.5	36
12	A Low-Complexity End-to-End Stereo Matching Pipeline From Raw Bayer Pattern Images to Disparity Maps. IEEE Access, 2021, 9, 47786-47794.	2.6	0
13	Fully Convolutional Network-Based DOA Estimation with Acoustic Vector Sensor. , 2021, , .		0
14	Spatial Non-Maximum Suppression for Object Detection using Correlation and Dynamic Thresholds. , 2021, , .		1
15	An Efficient CannyRaw Edge Detection Algorithm for Raw Images. , 2021, , .		0
16	Histogram of Oriented Gradients Feature Extraction From Raw Bayer Pattern Images. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 946-950.	2.2	49
17	Cascaded Form Sparse FIR Filter Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1692-1703.	3.5	6
18	Sparse FIR Filter Design Based on Cascaded Compensation Structure. , 2019, , .		5

#	ARTICLE	IF	CITATIONS
19	Design of Sparse FIR Filters With Reduced Effective Length. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1496-1506.	3.5	11
20	Sparse FIR Filter Design Based on Interpolation Technique. , 2018, , .		6
21	K-SVD Based Denoising Algorithm for DoFP Polarization Image Sensors. , 2018, , .		3
22	Investigation on power consumption of product accumulation block for multiplierless FIR filters. , 2017, , .		0
23	Low-Latency, Low-Area, and Scalable Systolic-Like Modular Multipliers for $GF(2^m)$ Based on Irreducible All-One Polynomials. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 399-408.	3.5	20
24	Lower Bound Analysis and Perturbation of Critical Path for Area-Time Efficient Multiple Constant Multiplications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 313-324.	1.9	11
25	Novel Structure for Area-Efficient Implementation of FIR Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1212-1216.	2.2	18
26	Low complexity and low power multiplierless FIR filter implementation. , 2017, , .		4
27	A passively compensated capacitive sensor readout with biased varactor temperature compensation and temperature coherent quantization. , 2017, , .		0
28	Design of Low-Power Multiplierless Linear-Phase FIR Filters. IEEE Access, 2017, 5, 23466-23472.	2.6	13
29	Analysis and Optimization of Product-Accumulation Section for Efficient Implementation of FIR Filters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1701-1713.	3.5	14
30	Fine-Grained Critical Path Analysis and Optimization for Area-Time Efficient Realization of Multiple Constant Multiplications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 863-872.	3.5	22
31	New Approach to the Reduction of Sign-Extension Overhead for Efficient Implementation of Multiple Constant Multiplications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2695-2705.	3.5	5
32	Fine-grained pipelining for multiple constant multiplications. , 2015, , .		3
33	Area-time efficient realization of multiple constant multiplication. , 2015, , .		1
34	High-speed multiplier block design based on bit-level critical path optimization. , 2014, , .		7