Nicola Petra

List of Publications by Year
in descending order

48 papers	1,301 citations	430874 18 h-index	377865 34 g-index
49 all docs	49 docs citations	49 times ranked	758 citing authors

#	Article	IF	Citations
1	Approximate Multipliers Based on New Approximate Compressors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 4169-4182.	5.4	171
2	Comparison and Extension of Approximate 4-2 Compressors for Low-Power Approximate Multipliers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3021-3034.	5.4	141
3	A 1.27 GHz, All-Digital Spread Spectrum Clock Generator/Synthesizer in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2010, 45, 1048-1060.	5.4	128
4	Truncated Binary Multipliers With Variable Correction and Minimum Mean Square Error. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1312-1325.	5.4	96
5	Design of Fixed-Width Multipliers With Linear Compensation Function. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 947-960.	5.4	57
6	Elementary Functions Hardware Implementation Using Constrained Piecewise-Polynomial Approximations. IEEE Transactions on Computers, 2011, 60, 418-432.	3.4	47
7	Efficient Logarithmic Converters for Digital Signal Processing Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 667-671.	3.0	44
8	Fixed-Width Multipliers and Multipliers-Accumulators With Min-Max Approximation Error. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2375-2388.	5.4	44
9	A 630 MHz, 76 mW Direct Digital Frequency Synthesizer Using Enhanced ROM Compression Technique. IEEE Journal of Solid-State Circuits, 2007, 42, 350-360.	5.4	43
10	High Speed Speculative Multipliers Based on Speculative Carry-Save Tree. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 3426-3435.	5.4	42
11	A 380 MHz Direct Digital Synthesizer/Mixer With Hybrid CORDIC Architecture in 0.25 $mu{hbox {m}}$ CMOS. IEEE Journal of Solid-State Circuits, 2007, 42, 151-160.	5.4	40
12	Reducing Lookup-Table Size in Direct Digital Frequency Synthesizers Using Optimized Multipartite Table Method. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 2116-2127.	5.4	40
13	High-Performance Special Function Unit for Programmable 3-D Graphics Processors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1968-1978.	5.4	40
14	Variable Latency Speculative Han-Carlson Adder. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1353-1361.	5.4	37
15	Direct Digital Frequency Synthesizer Using Nonuniform Piecewise-Linear Approximation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2409-2419.	5.4	25
16	Accurate Fixed-Point Logarithmic Converter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 526-530.	3.0	20
17	A Novel Architecture for Galois Fields GF(2^m) Multipliers Based on Mastrovito Scheme. IEEE Transactions on Computers, 2007, 56, 1470-1483.	3.4	19
18	On the use of approximate adders in carry-save multiplier-accumulators. , 2017, , .		19

#	Article	IF	Citations
19	Approximate Multipliers Using Static Segmentation: Error Analysis and Improvements. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2449-2462.	5.4	19
20	A 430 MHz, 280 mW Processor for the Conversion of Cartesian to Polar Coordinates in 0.25 $muhbox{m}$ CMOS. IEEE Journal of Solid-State Circuits, 2008, 43, 2503-2513.	5.4	18
21	A Standard-Cell-Based All-Digital PWM Modulator With High Resolution and Spread- Spectrum Capability. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3885-3896.	5.4	18
22	Digital Synthesizer/Mixer With Hybrid CORDICâ€“Multiplier Architecture: Error Analysis and Optimization. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 364-373.	5.4	17
23	Analytical Calculation of the Maximum Error for a Family of Truncated Multipliers Providing Minimum Mean Square Error. IEEE Transactions on Computers, 2011, 60, 1366-1371.	3.4	17
24	Low-Power Approximate Multiplier with Error Recovery using a New Approximate 4-2 Compressor. , 2020, , .		16
25	A novel truncated squarer with linear compensation function. , 2010, , .		15
26	A 3.3 GHz Spread-Spectrum Clock Generator Supporting Discontinuous Frequency Modulations in 28 nm CMOS. IEEE Journal of Solid-State Circuits, 2015, 50, 2074-2089.	5.4	15
27	Analysis and comparison of Direct Digital Frequency Synthesizers implemented on FPGA. The Integration VLSI Journal, 2014, 47, 261-271.	2.1	13
28	Design of fixed-width multipliers with minimum mean square error. , 2007, , .		11
29	A 41ps ASIC time-to-digital converter for physics experiments. Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2011, 659, 422-427.	1.6	10
30	Truncated squarer with minimum mean-square error. Microelectronics Journal, 2014, 45, 799-804.	2.0	10
31	On the Use of Approximate Multipliers in LMS Adaptive Filters. , 2018, , .		9
32	Efficient implementation of pseudochaotic piecewise linear maps with high digitization accuracies. International Journal of Circuit Theory and Applications, 2012, 40, 1-14.	2.0	8
33	FPGA Implementation of Gaussian Mixture Model Algorithm for 47â€‰fps Segmentation of 1080p Video. Journal of Electrical and Computer Engineering, 2013, 2013, 1-8.	0.9	8
34	Selfâ€tunable chaotic true random bit generator in currentâ€mode CMOS circuit with nonlinear distortion analysis. International Journal of Circuit Theory and Applications, 2019, 47, 1877-1892.	2.0	8
35	A Novel Module-Sign Low-Power Implementation for the DLMS Adaptive Filter With Low Steady-State Error. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 297-308.	5.4	6
36	A high performance floating-point special function unit using constrained piecewise quadratic approximation. , 2008, , .		5

#	Article	IF	Citations
37	A low-complexity programmable current mode circuit to design the sawtooth chaotic map. , 2017, , .		5
38	A 1.45 GHz All-Digital Spread Spectrum Clock Generator in 65nm CMOS for Synchronization-Free SoC Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3839-3852.	5.4	4
39	A high-speed and high-accuracy interpolator for digital modems. , 2008, , .		3
40	Single Flip-Flop Driving Circuit for Glitch-Free NAND-Based Digitally Controlled Delay-Lines. Circuits, Systems, and Signal Processing, 2017, 36, 1341-1360.	2.0	3
41	Constrained piecewise polinomial approximation for hardware implementation of elementary functions. , 2008, , .		2
42	Hardware performance versus video quality trade-off for Gaussian mixture model based background identification systems. , 2014, , .		2
43	High-speed differential resistor ladder for A/D converters. , 2010, , .		1
44	Stall-Aware Fixed-Point Implementation of LMS Filters. , 2018, , .		1
45	Variable-Rounded LMS Filter for Low-Power Applications. Lecture Notes in Electrical Engineering, 2020, , 155-161.	0.4	1
46	A Novel Low-Power High-Precision Implementation for Signâ€“Magnitude DLMS Adaptive Filters. Electronics (Switzerland), 2022, 11, 1007.	3.1	1
47	High Speed Galois Fields GF(2[?]) Multipliers. , 2007, , .		0
48	A novel low-power DLMS adaptive filter with sign-magnitude learning and approximated FIR section. , 2022, , .		0