Greg Stitt

List of Publications by Year
in descending order

24 papers	298 citations	1478505 6 h-index	1474206 9 g-index
24 all docs	24 docs citations	24 times ranked	257 citing authors

#	Article	IF	Citations
1	Scalable Performance Prediction of Irregular Workloads in Multi-Phase Particle-in-Cell Applications. , 2021, , .		0
2	Dynamic Scheduling on Heterogeneous Multicores. , 2019, , .		10
3	Multi-Parameter Performance Modeling using Symbolic Regression. , 2019, , .		4
4	Machine Learning-based Prediction for Dynamic, Runtime Architectural Optimizations of Embedded Systems. , 2019, , .		0
5	Machine Learning-based Prediction for Dynamic Architectural Optimizations. , 2019, , .		3
6	High-Frequency Absorption-FIFO Pipelining for Stratix 10 HyperFlex. , 2018, , .		0
7	Scalable Behavioral Emulation of Extreme-Scale Systems Using Structural Simulation Toolkit. , 2018, , .		11
8	A Uniquified Virtualization Approach to Hardware Security. IEEE Embedded Systems Letters, 2017, 9, 53-56.	1.9	7
9	Overlay-based side-channel countermeasures: A case study on correlated noise generation. , 2017, , .		1
10	A scheduling and binding heuristic for high-level synthesis of fault-tolerant FPGA applications. , 2015, , .		5
11	Fast, Flexible High-Level Synthesis from OpenCL using Reconfiguration Contexts. IEEE Micro, 2014, 34, 42-53.	1.8	23
12	A High Memory Bandwidth FPGA Accelerator for Sparse Matrix-Vector Multiplication. , 2014, , .		84
13	A comparison of correntropy-based feature tracking on FPGAs and GPUs. , 2013, , .		3
14	Pseudo-constant logic optimization. , 2013, , .		1
15	Virtual finite-state-machine architectures for fast compilation and portability. , 2013, , .		0
16	Bandwidth-Sensitivity-Aware Arbitration for FPGAs. IEEE Embedded Systems Letters, 2012, 4, 73-76.	1.9	4
17	High-Level Synthesis of In-Circuit Assertions for Verification, Debugging, and Timing Analysis. International Journal of Reconfigurable Computing, 2011, 2011, 1-17.	0.2	17
18	Intermediate Fabrics: Virtual Architectures for Near-Instant FPGA Compilation. IEEE Embedded Systems Letters, 2011, 3, 81-84.	1.9	30

#	Article	IF	Citations
19	Novo-G: At the Forefront of Scalable Reconfigurable Supercomputing. Computing in Science and Engineering, 2011, 13, 82-86.	1.2	60
20	Are Field-Programmable Gate Arrays Ready for the Mainstream?. IEEE Micro, 2011, 31, 58-63.	1.8	16
21	An End-to-End Tool Flow for FPGA-Accelerated Scientific Computing. IEEE Design and Test of Computers, 2011, 28, 68-77.	1.0	2
22	Traversal Caches: A Framework for FPGA Acceleration of Pointer Data Structures. International Journal of Reconfigurable Computing, 2010, 2010, 1-16.	0.2	4
23	A scalable performance prediction heuristic for implementation planning on heterogeneous systems. , 2010, , .		2
24	A Traversal Cache Framework for FPGA Acceleration of Pointer Data Structures: A Case Study on Barnes-Hut N-body Simulation. , 2009, , .		11