Shuai Wang

List of Publications by Year
in descending order

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15	79	2682572	2550090
papers	citations	2	3
		h-index	g-index

15	15	15	84
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Visual and Phonological Feature Enhanced Siamese BERT for Chinese Spelling Error Correction. Applied Sciences (Switzerland), 2022, 12, 4578.	2.5	0
2	Low Power Aging-Aware On-Chip Memory Structure Design by Duty Cycle Balancing. Journal of Circuits, Systems and Computers, 2016, 25, 1650115.	1.5	1
3	Exploiting narrow-width values for improving non-volatile cache lifetime. , 2014, , .		7
4	Exploiting narrow-width values for improving non-volatile cache lifetime. , 2014, , .		3
5	Characterizing soft error vulnerability of cache coherence protocols for chip-multiprocessors. , 2014, , .		0
6	Wireless networkâ€onâ€chip: a survey. Journal of Engineering, 2014, 2014, 98-104.	1.1	23
7	1-to-Many and many-to-1 communication in hybrid wireless network-on-chip. , 2013, , .		0
8	Parallelized Near-Duplicate Document Detection Algorithm for Large Scale Chinese Web Pages. , 2012, , .		0
9	Low power aging-aware register file design by duty cycle balancing. , 2012, , .		1
10	Aging-Aware Instruction Cache Design by Duty Cycle Balancing. , 2012, , .		9
11	Software reliability estimation method based on Markov usage models using Importance Sampling. , 2012, , .		2
12	Replicating Tag Entries for Reliability Enhancement in Cache Tag Arrays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 643-654.	3.1	23
13	Exploring hardware transaction processing for reliable computing in chip-multiprocessors against soft errors. , 2012, , .		0
14	Characterizing the L1 Data Cache's Vulnerability to Transient Errors in Chip-Multiprocessors. , 2011, , .		5
15	Characterizing System-Level Vulnerability for Instruction Caches against Soft Errors. , 2011, , .		5