Sanjukta Bhanja

List of Publications by Year
in descending order

50 papers	656 citations	1040056 9 h-index	888059 17 g-index
50 all docs	50 docs citations	50 times ranked	482 citing authors

#	Article	IF	Citations
1	QCAPro - An error-power estimation tool for QCA circuit design. , 2011, , .		189
2	MRAM PUF: A Novel Geometry Based Magnetic PUF With Integrated CMOS. IEEE Nanotechnology Magazine, 2015, 14, 436-443.	2.0	70
3	Low Power Magnetic Quantum Cellular Automata Realization Using Magnetic Multi-Layer Structures. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 267-276.	3.6	47
4	Non-Boolean computing with nanomagnets for computer vision applications. Nature Nanotechnology, 2016, 11, 177-183.	31.5	47
5	QCA Circuits for Robust Coplanar Crossing. Journal of Electronic Testing: Theory and Applications (JETTA), 2007, 23, 193-210.	1.2	40
6	Probabilistic Modeling of QCA Circuits Using Bayesian Networks. IEEE Nanotechnology Magazine, 2006, 5, 657-670.	2.0	35
7	Hierarchical Probabilistic Macromodeling for QCA Circuits. IEEE Transactions on Computers, 2007, 56, 174-190.	3.4	33
8	Landauer Clocking for Magnetic Cellular Automata (MCA) Arrays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 714-717.	3.1	22
9	Study of single layer and multilayer nano-magnetic logic architectures. Journal of Applied Physics, 2012, 111, 07A928.	2.5	21
10	Reliability of bi-stable single domain nano magnets for Cellular Automata. , 2007, , .		14
11	Sequential Circuit Design in Quantum-Dot Cellular Automata. , 2008, , .		14
12	Study of Dipolar Neighbor Interaction on Magnetization States of Nano-Magnetic Disks. IEEE Transactions on Magnetics, 2013, 49, 3129-3132.	2.1	14
13	A Novel Transverse Read Technique for Domain-Wall â€œRacetrackâ€•Memories. IEEE Nanotechnology Magazine, 2020, 19, 648-652.	2.0	10
14	A novel geometry based MRAM PUF. , 2014, , .		9
15	Study of magnetization state transition in closely spaced nanomagnet two-dimensional array for computation. Journal of Applied Physics, 2011, 109, 07E513.	2.5	8
16	Error-Power Tradeoffs in QCA Design. , 2008, , .		7
17	Non-destructive variability tolerant differential read for non-volatile logic. , 2012, , .		7
18	Nano Magnetic STT-Logic Partitioning for Optimum Performance. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 90-98.	3.1	7

#	Article	IF	Citations
19	Direct Quadratic Minimization Using Magnetic Field-Based Computing. , 2008, , .		6
20	A review of magnetic cellular automata systems. , 2011, , .		6
21	Magnetic State Estimator to Characterize the Magnetic States of Nano-Magnetic Disks. IEEE Transactions on Magnetics, 2013, 49, 3545-3548.	2.1	5
22	Toward Comprehensive Shifting Fault Tolerance for Domain-Wall Memories With PIETT. IEEE Transactions on Computers, 2023, 72, 1095-1109.	3.4	5
23	Defect characterization in magnetic field coupled arrays. , 2009, , .		4
24	Low power CMOS-magnetic nano-logic with increased bit controllability. , 2011, , .		4
25	Reading Nanomagnetic Energy Minimizing Coprocessor. IEEE Nanotechnology Magazine, 2018, 17, 368-372.	2.0	4
26	Integrating a Nanologic Knowledge Module Into an Undergraduate Logic Design Course. IEEE Transactions on Education, 2008, 51, 349-355.	2.4	3
27	Magnetic Cellular Automata (MCA) arrays under spatially varying field. , 2009, , .		3
28	An experimental demonstration of the viability of energy minimizing computing using nano-magnets. , 2011, , .		3
29	Addressing the layout constraint problem when cascading logic gates in nanomagnetic logic. , 2012, , .		3
30	A novel design concept for high density hybrid CMOS-nanomagnetic circuits. , 2012, , .		3
31	Probabilistic error modeling for sequential logic. , 2007, , .		2
32	Driving magnetic cells for information storage and propagation. , 2010, , .		2
33	Variability tolerant reading of nanomagnetic energy minimizing co-processor. , 2017, , .		2
34	Integrating Nano-logic into an Undergraduate Logic Design Course. , 2007, , .		1
35	Selective Redundancy: Evaluation of Temporal Reliability Enhancement Scheme for Nanoelectronic Circuits. , 2008, , .		1
36	Work in progress - an education module on engineering ethics concentrating on environment-friendly engineering for computer engineers. , 2009, , .		1

#	Article	IF	Citations
37	Evaluation of circuit styles and VLSI logic designs of pentacene OTFTs. , 2012, , .		1
38	A novel knowledge module to integrate threshold logic and post-CMOS technology into undergraduate logic design classroom. , 2014, , .		1
39	Exploring the readability of nano-magnetic energy minimizing co-processor. , 2017, , .		1
40	Pinning Fault Mode Modeling for DWM Shifting. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3319-3323.	3.0	1
41	Work in Progress: Dominant Sensory Mode based Groups in VLSI Classes. , 2006, , .		0
42	Work in progress - Introduction of K-map based nano-logic synthesis as knowledge module in logic design course. Proceedings - Frontiers in Education Conference, FIE, 2007, , .	0.0	0
43	CNT logic knowledge module integrated in digital CMOS logic design course. , 2009, , .		0
44	Tool for analysis and quantification of fabrication layouts in nanomagnet-based computing. , 2011, , .		0
45	Effectiveness of Knowledge Module on “Intel 45 nm transistor and high-k dielectric” into undergraduate semiconductor devices course. , 2012, , .		0
46	Prospects for pipeline in high-density magnetic field-coupled logic. , 2014, , .		0
47	Integrating emerging memory technologies into undergraduate logic design course: The impact of context based teaching. , 2017, , .		0
48	Structural Study of MgO Barrier Layer in Magnetic Devices for Computing. , 2018, , .		0
49	A Study on Reconfigurable Nanomagnetic Array and Effect of Gilbert Damping on Reconfigurability. IEEE Nanotechnology Magazine, 2021, 20, 503-506.	2.0	0
50	XDWM: A 2D Domain Wall Memory. IEEE Nanotechnology Magazine, 2022, , 1-1.	2.0	0