Juan Antonio Maestro

List of Publications by Year
in descending order

172	2,364	279798	345221
papers	citations	23 h-index	36 g-index

174	174	174	1155
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	ACME-2: Improving the Extraction of Essential Bits in Xilinx SRAM-Based FPGAs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1577-1581.	3.0	1
2	A new radiation-hardened architecture for holographic memory address calculation. AEJ - Alexandria Engineering Journal, 2022, 61, 6181-6190.	6.4	0
3	An analysis of FPGA configuration memory SEU accumulation and a preventative scrubbing technique. Microprocessors and Microsystems, 2022, 90, 104467.	2.8	2
4	Flexible and area-efficient Galois field Arithmetic Logic Unit for soft-core processors. Computers and Electrical Engineering, 2022, 99, 107759.	4.8	3
5	RISC-V Galois Field ISA Extension for Non-Binary Error-Correction Codes and Classical and Post-Quantum Cryptography. IEEE Transactions on Computers, 2022, , 1-1.	3.4	5
6	Low delay non-binary error correction codes based on Orthogonal Latin Squares. The Integration VLSI Journal, 2021, 76, 55-60.	2.1	1
7	Decoding Algorithm for Quadruple-Error-Correcting Reed-Solomon Codes and Its Derived Architectures. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1438-1442.	3.0	0
8	Fault Injection Emulation for Systems in FPGAs: Tools, Techniques and Methodology, a Tutorial. Sensors, 2021, 21, 1392.	3.8	5
9	Reliability Analysis of ASIC Designs With Xilinx SRAM-Based FPGAs. IEEE Access, 2021, 9, 140676-140685.	4.2	2
10	Reliability Analysis of the SHyLoC CCSDS123 IP Core for Lossless Hyperspectral Image Compression Using COTS FPGAs. Electronics (Switzerland), 2020, 9, 1681.	3.1	6
11	A Methodology to Analyze the Fault Tolerance of Demosaicking Methods against Memory Single Event Functional Interrupts (SEFIs). Electronics (Switzerland), 2020, 9, 1619.	3.1	2
12	Efficient Majority-Logic Reed-Solomon Decoders for Single Symbol Correction. IEEE Transactions on Device and Materials Reliability, 2020, 20, 390-394.	2.0	1
13	Radiation Hardened Digital Direct Synthesizer With CORDIC for Spaceborne Applications. IEEE Access, 2020, 8, 83167-83176.	4.2	7
14	Toward a Fault-Tolerant Star Tracker for Small Satellite Applications. IEEE Transactions on Aerospace and Electronic Systems, 2020, 56, 3421-3431.	4.7	7
15	An Algorithmic-Based Fault Detection Technique for the 1-D Discrete Cosine Transform. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1336-1340.	3.1	3
16	Combined symbol error correction and spare through-silicon vias for 3D memories. IEEE Transactions on Emerging Topics in Computing, 2020, , 1-1.	4.6	1
17	Analysis of the Critical Bits of a RISC-V Processor Implemented in an SRAM-Based FPGA for Space Applications. Electronics (Switzerland), 2020, 9, 175.	3.1	22
18	Low-Latency and Low-Power Test-Vector Selector for Reed-Solomonâ€™s Low-Complexity Chase. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3362-3366.	3.0	0

#	Article	IF	Citations
19	Analyzing the impact of the Operating System on the Reliability of a RISC-V FPGA Implementation. , 2020, , .		7
20	Reduction of Parity Overhead in a Subset of Orthogonal Latin Square Codes. , 2020, , .		1
21	Protection Scheme for Star Tracker Images. IEEE Transactions on Aerospace and Electronic Systems, 2019, 55, 486-492.	4.7	4
22	Enhanced Limited Magnitude Error Correcting Codes for Multilevel Cell Main Memories. IEEE Nanotechnology Magazine, 2019, 18, 1023-1026.	2.0	3
23	ACME: A Tool to Improve Configuration Memory Fault Injection in SRAM-Based FPGAs. IEEE Access, 2019, 7, 128153-128161.	4.2	23
24	An ALU Protection Methodology for Soft Processors on SRAM-Based FPGAs. IEEE Transactions on Computers, 2019, 68, 1404-1410.	3.4	20
25	A Scheme to Design Concurrent Error Detection Techniques for the Fast Fourier Transform Implemented in SRAM-Based FPGAs. IEEE Transactions on Computers, 2018, 67, 1039-1045.	3.4	11
26	Evaluating the Impact of the Instruction Set on Microprocessor Reliability to Soft Errors. IEEE Transactions on Device and Materials Reliability, 2018, 18, 70-79.	2.0	19
27	Majority Voting-Based Reduced Precision Redundancy Adders. IEEE Transactions on Device and Materials Reliability, 2018, 18, 122-124.	2.0	20
28	Fault tolerant encoders for Single Error Correction and Double Adjacent Error Correction codes. Microelectronics Reliability, 2018, 81, 167-173.	1.7	6
29	A Fast Technique to Reduce Power Consumption on Linear Block Codes Used to Protect Registers. IEEE Transactions on Device and Materials Reliability, 2018, 18, 189-196.	2.0	1
30	An Efficient Methodology for On-Chip SEU Injection in Flip-Flops for Xilinx FPGAs. IEEE Transactions on Nuclear Science, 2018, 65, 989-996.	2.0	19
31	Modular fault tolerant processor architecture on a SoC for space. Microelectronics Reliability, 2018, 83, 84-90.	1.7	3
32	Efficient Fault-Tolerant Design for Parallel Matched Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 366-370.	3.0	7
33	A Comparison of Dual Modular Redundancy and Concurrent Error Detection in Finite Impulse Response Filters Implemented in SRAM-Based FPGAs Through Fault Injection. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 376-380.	3.0	4
34	An Efficient Fault-Tolerance Design for Integer Parallel Matrixâ€“Vector Multiplications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 211-215.	3.1	3
35	Reducing the Power Consumption of Fault Tolerant Registers Through Hybrid Protection. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1293-1302.	5.4	4
36	Efficient Protection of the Register File in Soft-Processors Implemented on Xilinx FPGAs. IEEE Transactions on Computers, 2018, 67, 299-304.	3.4	15

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37	Protecting Image Processing Pipelines against Configuration Memory Errors in SRAM-Based FPGAs. Electronics (Switzerland), 2018, 7, 322.	3.1	4
38	Multiple Cell Upset Injection in BRAMs for Xilinx FPGAs. IEEE Transactions on Device and Materials Reliability, 2018, 18, 636-638.	2.0	5
39	Enhancing Instruction TLB Resilience to Soft Errors. IEEE Transactions on Computers, 2018, , 1-1.	3.4	4
40	Seu and Sefi error detection and correction on a ddr3 memory system. Microelectronics Reliability, 2018, 91, 23-30.	1.7	1
41	Comments on â€œExtend orthogonal Latin square codes for 32-bit data protection in memory applicationsâ€•Microelectron. Reliab. 63, 278â€“283 (2016). Microelectronics Reliability, 2017, 69, 126-129.	1.7	1
42	Combined Modular Key and Data Error Protection for Content-Addressable Memories. IEEE Transactions on Computers, 2017, 66, 1085-1090.	3.4	4
43	A Scheme to Reduce the Number of Parity Check Bits in Orthogonal Latin Square Codes. IEEE Transactions on Reliability, 2017, 66, 518-528.	4.6	7
44	Error Detection Technique for a Median Filter. IEEE Transactions on Nuclear Science, 2017, , 1-1.	2.0	16
45	A method to protect Cuckoo filters from soft errors. Microelectronics Reliability, 2017, 72, 85-89.	1.7	0
46	Single Event Transient Tolerant Bloom Filter Implementations. IEEE Transactions on Computers, 2017, 66, 1831-1836.	3.4	11
47	A method to recover critical bits under a double error in SEC-DED protected memories. Microelectronics Reliability, 2017, 73, 92-96.	1.7	5
48	Characterizing a RISC-V SRAM-based FPGA implementation against Single Event Upsets using fault injection. Microelectronics Reliability, 2017, 78, 205-211.	1.7	22
49	A Scheme to Improve the Intrinsic Error Detection of the Instruction Set Architecture. IEEE Computer Architecture Letters, 2017, 16, 103-106.	1.5	12
50	SEFI Protection for Nanosat 16-Bit Chip Onboard Computer Memories. IEEE Transactions on Device and Materials Reliability, 2017, 17, 698-707.	2.0	11
51	A novel concurrent error detection technique for the fast Fourier transform implemented in SRAM-based FPGAs. , 2016, , .		2
52	Efficient fault tolerant parallel matrix-vector multiplications. , 2016, , .		2
53	Efficient implementation of single event upset tolerant register comparison. Electronics Letters, 2016, 52, 1922-1923.	1.0	0
54	Improving counting Bloom filter performance with fingerprints. Information Processing Letters, 2016, 116, 304-309.	0.6	26

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55	Reducing the Cost of Triple Adjacent Error Correction in Double Error Correction Orthogonal Latin Square Codes. IEEE Transactions on Device and Materials Reliability, 2016, 16, 269-271.	2.0	7
56	Unequal error protection codes derived from SECâ€ÐED codes. Electronics Letters, 2016, 52, 619-620.	1.0	7
57	DMR+: An efficient alternative to TMR to protect registers in Xilinx FPGAs. Microelectronics Reliability, 2016, 63, 314-318.	1.7	3
58	Combined SEU and SEFI Protection for Memories Using Orthogonal Latin Square Codes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1933-1943.	5.4	16
59	A fault-tolerant implementation of the median filter. , 2016, , .		5
60	Optimizing the Implementation of SECâ€“DAEC Codes in FPGAs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3538-3542.	3.1	4
61	Implementing Double Error Correction Orthogonal Latin Squares Codes in SRAM-based FPGAs. Microelectronics Reliability, 2016, 56, 221-227.	1.7	6
62	Unequal Error Protection Codes Derived from Double Error Correction Orthogonal Latin Square Codes. IEEE Transactions on Computers, 2016, 65, 2932-2938.	3.4	5
63	Oddâ€weightâ€column SECâ€“DEDâ€“TAED codes. Electronics Letters, 2016, 52, 119-120.	1.0	3
64	A Method to Design Single Error Correction Codes With Fast Decoding for a Subset of Critical Bits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 171-175.	3.0	10
65	An Efficient Single and Double-Adjacent Error Correcting Parallel Decoder for the (24,12) Extended Golay Code. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1603-1606.	3.1	28
66	A Comment on â€œFast Bloom Filters and Their Generalizationâ€ IEEE Transactions on Parallel and Distributed Systems, 2016, 27, 303-304.	5.6	11
67	Parallel d-Pipeline: A Cuckoo Hashing Implementation for Increased Throughput. IEEE Transactions on Computers, 2016, 65, 326-331.	3.4	23
68	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 769-773.	3.1	21
69	Efficient Coding Schemes for Fault-Tolerant Parallel Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 666-670.	3.0	9
70	A method to protect Bloom filters from soft errors. , 2015, , .		5
71	Efficient error detection in multiple way tables. Electronics Letters, 2015, 51, 50-52.	1.0	0
72	MCU Tolerance in SRAMs Through Low-Redundancy Triple Adjacent Error Correction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2332-2336.	3.1	53

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73	Fault Tolerant Parallel Filters Based on Error Correction Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 384-387.	3.1	32
74	A Synergetic Use of Bloom Filters for Error Detection and Correction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 584-587.	3.1	10
75	Low Delay Single Symbol Error Correction Codes Based on Reed Solomon Codes. IEEE Transactions on Computers, 2015, 64, 1497-1501.	3.4	30
76	A Class of SEC-DED-DAEC Codes Derived From Orthogonal Latin Square Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 968-972.	3.1	23
77	FastTag: A Technique to Protect Cache Tags Against Soft Errors. IEEE Transactions on Device and Materials Reliability, 2014, 14, 935-937.	2.0	14
78	Implementing error detection in fast counting Bloom filters. Electronics Letters, 2014, 50, 1602-1604.	1.0	1
79	A Method to Design SEC-DED-DAEC Codes With Optimized Decoding. IEEE Transactions on Device and Materials Reliability, 2014, 14, 884-889.	2.0	36
80	Hamming SEC-DAED and Extended Hamming SEC-DED-TAED Codes Through Selective Shortening and Bit Placement. IEEE Transactions on Device and Materials Reliability, 2014, 14, 574-576.	2.0	57
81	An experimental power profile of Energy Efficient Ethernet switches. Computer Communications, 2014, 50, 110-118.	5.1	6
82	Energy Efficient Exact Matching for Flow Identification with Cuckoo Affinity Hashing. IEEE Communications Letters, 2014, 18, 885-888.	4.1	6
83	Optimized parallel decoding of difference set codes for high speed memories. Microelectronics Reliability, 2014, 54, 2645-2648.	1.7	3
84	Efficient Flow Sampling With Back-Annotated Cuckoo Hashing. IEEE Communications Letters, 2014, 18, 1695-1698.	4.1	3
85	A Method to Extend Orthogonal Latin Square Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1635-1639.	3.1	15
86	Exploiting processor features to implement error detection in reduced precision matrix multiplications. Microprocessors and Microsystems, 2014, 38, 581-584.	2.8	5
87	A fault tolerant implementation of the Goertzel algorithm. Microelectronics Reliability, 2014, 54, 335-337.	1.7	2
88	Efficient implementation of error correction codes in hash tables. Microelectronics Reliability, 2014, 54, 338-340.	1.7	3
89	Error Detection in Majority Logic Decoding of Euclidean Geometry Low Density Parity Check (EG-LDPC) Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 156-159.	3.1	34
90	A Method to Construct Low Delay Single Error Correction Codes for Protecting Data Bits Only. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 479-483.	2.7	42

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91	Reducing the Cost of Single Error Correction With Parity Sharing. IEEE Transactions on Device and Materials Reliability, 2013, 13, 420-422.	2.0	4
92	Efficient single event upset-tolerant FIR filter design based on residue number for OBP satellite communication systems. China Communications, 2013, 10, 55-67.	3.2	5
93	Enhanced Duplication: a Technique to Correct Soft Errors in Narrow Values. IEEE Computer Architecture Letters, 2013, 12, 13-16.	1.5	3
94	Low Complexity Concurrent Error Detection for Complex Multiplication. IEEE Transactions on Computers, 2013, 62, 1899-1903.	3.4	11
95	An Efficient Technique to Protect Serial Shift Registers Against Soft Errors. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 512-516.	3.0	4
96	Soft error tolerant Content Addressable Memories (CAMs) using error detection codes and duplication. Microprocessors and Microsystems, 2013, 37, 1103-1107.	2.8	3
97	Efficient Arithmetic-Residue-Based SEU-Tolerant FIR Filter Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 497-501.	3.0	13
98	Using Single Error Correction Codes to Protect Against Isolated Defects and Soft Errors. IEEE Transactions on Reliability, 2013, 62, 238-243.	4.6	8
99	Concurrent Error Detection for Orthogonal Latin Squares Encoders and Syndrome Computation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 2334-2338.	3.1	20
100	Optimised decoding of oddâ€weight single error correction double error detection codes with 64 bits. Electronics Letters, 2013, 49, 1617-1618.	1.0	2
101	Reducing the Cost of Implementing Error Correction Codes in Content Addressable Memories. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 432-436.	3.0	6
102	Diverse Double Modular Redundancy: A New Direction for Soft-Error Detection and Correction. IEEE Design and Test, 2013, 30, 87-95.	1.2	24
103	Verification of SRAM MСUs calculation technique for experiment time optimization. , 2013, , .		3
104	Study of the potential energy savings in Ethernet by combining Energy Efficient Ethernet and Adaptive Link Rate. European Transactions on Telecommunications, 2012, 23, 227-233.	1.2	10
105	Area efficient concurrent error detection and correction for parallel filters. Electronics Letters, 2012, 48, 1258.	1.0	17
106	Low-cost single error correction multiple adjacent error correction codes. Electronics Letters, 2012, 48, 1470.	1.0	10
107	A (64,45) Triple Error Correction Code for Memory Applications. IEEE Transactions on Device and Materials Reliability, 2012, 12, 101-106.	2.0	20
108	Comparison of the Susceptibility to Soft Errors of SRAM-Based FPGA Error Correction Codes Implementations. IEEE Transactions on Nuclear Science, 2012, 59, 619-624.	2.0	12

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109	Network monitoring for energy efficiency in large-scale networks: the case of the Spanish Academic Network. Journal of Supercomputing, 2012, 62, 1284-1304.	3.6	1
110	Implementing Concurrent Error Detection in Infinite-Impulse-Response Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 583-586.	3.0	5
111	Low Power embedded DRAM caches using BCH code partitioning. , 2012, , .		7
112	Enhanced Detection of Double and Triple Adjacent Errors in Hamming Codes Through Selective Bit Placement. IEEE Transactions on Device and Materials Reliability, 2012, 12, 357-362.	2.0	44
113	Efficient error detection in Double Error Correction BCH codes for memory applications. Microelectronics Reliability, 2012, 52, 1528-1530.	1.7	26
114	Multiple Cell Upset Correction in Memories Using Difference Set Codes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 2592-2599.	5.4	32
115	On the Use of Euclidean Geometry Codes for Efficient Multibit Error Correction on Memory Systems. IEEE Transactions on Nuclear Science, 2012, 59, 824-828.	2.0	6
116	Error-Detection Enhanced Decoding of Difference Set Codes for Memory Applications. IEEE Transactions on Device and Materials Reliability, 2012, 12, 335-340.	2.0	9
117	Efficient Majority Logic Fault Detection With Difference-Set Codes for Memory Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 148-156.	3.1	62
118	Validation and optimization of TMR protections for circuits in radiation environments. , 2011, , .		1
119	Structural DMR: A Technique for Implementation of Soft-Error-Tolerant FIR Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 512-516.	3.0	27
120	Increasing Reliability of FPGA-Based Adaptive Equalizers in the Presence of Single Event Upsets. IEEE Transactions on Nuclear Science, 2011, 58, 1072-1077.	2.0	17
121	Improving Memory Reliability Against Soft Errors Using Block Parity. IEEE Transactions on Nuclear Science, 2011, 58, 981-986.	2.0	15
122	Mitigating the effects of large multiple cell upsets (MCUs) in memories. ACM Transactions on Design Automation of Electronic Systems, 2011, 16, 1-10.	2.6	3
123	A fast and efficient technique to apply Selective TMR through optimization. Microelectronics Reliability, 2011, 51, 2388-2401.	1.7	8
124	Improving Energy Efficiency in IEEE 802.3ba High-Rate Ethernet Optical Links. IEEE Journal of Selected Topics in Quantum Electronics, 2011, 17, 419-427.	2.9	10
125	An Initial Evaluation of Energy Efficient Ethernet. IEEE Communications Letters, 2011, 15, 578-580.	4.1	76
126	Offset DMR: A Low Overhead Soft Error Detection and Correction Technique for Transform-Based Convolution. IEEE Transactions on Computers, 2011, 60, 1511-1516.	3.4	4

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127	Fault Tolerant Single Error Correction Encoders. Journal of Electronic Testing: Theory and Applications (JETTA), 2011, 27, 215-218.	1.2	13
128	Mitigation of permanent faults in adaptive equalizers. Microelectronics Reliability, 2011, 51, 703-710.	1.7	1
129	Towards an energy efficient 10 Gb/s optical ethernet: Performance analysis and viability. Optical Switching and Networking, 2011, 8, 131-138.	2.0	23
130	Low-complexity Concurrent Error Detection for convolution with Fast Fourier Transforms. Microelectronics Reliability, 2011, 51, 1152-1156.	1.7	0
131	On the expected longest length probe sequence for hashing with separate chaining. Journal of Discrete Algorithms, 2011, 9, 307-312.	0.7	3
132	Designing ad-hoc scrubbing sequences to improve memory reliability against soft errors. , 2011, , .		1
133	Signal shaping dual modular redundancy for soft error tolerant finite impulse response filters. Electronics Letters, 2011, 47, 1272.	1.0	9
134	Reliability analysis of memories protected with BICS and a per-word parity bit. ACM Transactions on Design Automation of Electronic Systems, 2010, 15, 1-15.	2.6	5
135	Very-low-complexity concurrent error detection for transform-based filters. Electronics Letters, 2010, 46, 1677.	1.0	0
136	Enhanced Implementations of Hamming Codes to Protect FIR Filters. IEEE Transactions on Nuclear Science, 2010, 57, 2112-2118.	2.0	6
137	Matrix-Based Codes for Adjacent Error Correction. IEEE Transactions on Nuclear Science, 2010, 57, 2106-2111.	2.0	37
138	IEEE 802.3az: the road to energy efficient ethernet. , 2010, 48, 50-56.		255
139	Burst Transmission in Energy Efficient Ethernet. IEEE Internet Computing, 2010, , .	3.3	51
140	Energy Efficiency in Industrial Ethernet: The Case of Powerlink. IEEE Transactions on Industrial Electronics, 2010, 57, 2896-2903.	7.9	27
141	Number of Events and Time to Failure Distributions for Error Correction Protected Memories. IEEE Transactions on Device and Materials Reliability, 2010, 10, 381-389.	2.0	3
142	Optimizing Scrubbing Sequences for Advanced Computer Memories. IEEE Transactions on Device and Materials Reliability, 2010, 10, 192-200.	2.0	11
143	Protection of Memories Suffering MCUs Through the Selection of the Optimal Interleaving Distance. IEEE Transactions on Nuclear Science, 2010, 57, 2124-2128.	2.0	38
144	Efficient Soft Error-Tolerant Adaptive Equalizers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2032-2040.	5.4	11

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145	Soft error detection and correction for FFT based convolution using different block lengths. , 2009, , .		3
146	Selection of the optimal interleaving distance for memories suffering MCUs. , 2009, , .		0
147	Reliability of Single-Error Correction Protected Memories. IEEE Transactions on Reliability, 2009, 58, 193-201.	4.6	21
148	A method to eliminate the event accumulation problem from a memory affected by multiple bit upsets. Microelectronics Reliability, 2009, 49, 707-715.	1.7	4
149	Protection against soft errors in the space environment: A finite impulse response (FIR) filter case study. The Integration VLSI Journal, 2009, 42, 128-136.	2.1	6
150	Efficient error detection codes for multiple-bit upset correction in SRAMs with BICS. ACM Transactions on Design Automation of Electronic Systems, 2009, 14, 1-10.	2.6	14
151	A Methodology for Automatic Insertion of Selective TMR in Digital Circuits Affected by SEUs. IEEE Transactions on Nuclear Science, 2009, 56, 2091-2102.	2.0	55
152	Fault tolerant FIR filters using hamming codes. , 2009, , .		3
153	Performance evaluation of energy efficient ethernet. IEEE Communications Letters, 2009, 13, 697-699.	4.1	112
154	Study of the Effects of Multibit Error Correction Codes on the Reliability of Memories in the Presence of MBUs. IEEE Transactions on Device and Materials Reliability, 2009, 9, 31-39.	2.0	21
155	Selection of the Optimal Memory Configuration in a System Affected by Soft Errors. IEEE Transactions on Device and Materials Reliability, 2009, 9, 403-411.	2.0	10
156	Fault Tolerance Analysis of Communication System Interleavers: the 802.11a Case Study. Journal of Signal Processing Systems, 2008, 52, 231-247.	2.1	0
157	Study of the effects of MBUs on the reliability of a 150 nm SRAM device. , 2008, , .		22
158	Efficient Protection Techniques Against SEUs for Adaptive Filters: An Echo Canceller Case Study. IEEE Transactions on Nuclear Science, 2008, 55, 1700-1707.	2.0	18
159	A technique to calculate the MBU distribution of a memory under radiation suffering the event accumulation problem. , 2008, , .		7
160	A new EDAC technique against soft errors based on pulse detectors. , 2008, , .		3
161	Performance analysis and improvements for a simulation-based fault injection platform. , 2008, , .		8
162	A Simulation Platform for the Study of Soft Errors on Signal Processing Circuits through Software Fault Injection. , 2007, , .		16

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163	System knowledge-based techniques against SEUs for adaptive filters. , 2007, , .		1
164	Reliability Analysis of Memories Suffering Multiple Bit Upsets. IEEE Transactions on Device and Materials Reliability, 2007, 7, 592-601.	2.0	57
165	An Experimental Analysis of SEU Sensitiveness on System Knowledge-based Hardening Techniques. , 2007, , .		3
166	New Protection Techniques Against SEUs for Moving Average Filters in a Radiation Environment. IEEE Transactions on Nuclear Science, 2007, 54, 957-964.	2.0	28
167	A New Protection Technique for Finite Impulse Response (FIR) Filters in the Presence of Soft Errors. , 2007, , .		7
168	New Alternatives to the Estimation Problem in Hardware-Software Codesign of Complex Embedded Systems: The H.261 Video Co-dec Case Study. Design Automation for Embedded Systems, 2004, 9, 193-210.	1.0	0
169	A grouping partitioning technique with automatic criterion selection for the codesign process. , 0, , .		0
170	A macroscopic time and cost estimation model allowing task parallelism and hardware sharing for the codesign partitioning process. , 0, , .		4
171	The heterogeneous structure problem in hardware/software codesign: a macroscopic approach. , 0, , .		0
172	Energy Efficiency in Ethernet. , 0, , 277-290.		0