Juan Antonio Maestro

List of Publications by Year
in descending order

172	2,364	279487 23	344852 36
papers	citations	h-index	g-index

174	174	174	1155
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	IEEE 802.3az: the road to energy efficient ethernet. , 2010, 48, 50-56.		255
2	Performance evaluation of energy efficient ethernet. IEEE Communications Letters, 2009, 13, 697-699.	2.5	112
3	An Initial Evaluation of Energy Efficient Ethernet. IEEE Communications Letters, 2011, 15, 578-580.	2.5	76
4	Efficient Majority Logic Fault Detection With Difference-Set Codes for Memory Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 148-156.	2.1	62
5	Reliability Analysis of Memories Suffering Multiple Bit Upsets. IEEE Transactions on Device and Materials Reliability, 2007, 7, 592-601.	1.5	57
6	Hamming SEC-DAED and Extended Hamming SEC-DED-TAED Codes Through Selective Shortening and Bit Placement. IEEE Transactions on Device and Materials Reliability, 2014, 14, 574-576.	1.5	57
7	A Methodology for Automatic Insertion of Selective TMR in Digital Circuits Affected by SEUs. IEEE Transactions on Nuclear Science, 2009, 56, 2091-2102.	1.2	55
8	MCU Tolerance in SRAMs Through Low-Redundancy Triple Adjacent Error Correction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2332-2336.	2.1	53
9	Burst Transmission in Energy Efficient Ethernet. IEEE Internet Computing, 2010, , .	3.2	51
10	Enhanced Detection of Double and Triple Adjacent Errors in Hamming Codes Through Selective Bit Placement. IEEE Transactions on Device and Materials Reliability, 2012, 12, 357-362.	1.5	44
11	A Method to Construct Low Delay Single Error Correction Codes for Protecting Data Bits Only. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 479-483.	1.9	42
12	Protection of Memories Suffering MCUs Through the Selection of the Optimal Interleaving Distance. IEEE Transactions on Nuclear Science, 2010, 57, 2124-2128.	1.2	38
13	Matrix-Based Codes for Adjacent Error Correction. IEEE Transactions on Nuclear Science, 2010, 57, 2106-2111.	1.2	37
14	A Method to Design SEC-DED-DAEC Codes With Optimized Decoding. IEEE Transactions on Device and Materials Reliability, 2014, 14, 884-889.	1.5	36
15	Error Detection in Majority Logic Decoding of Euclidean Geometry Low Density Parity Check (EG-LDPC) Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 156-159.	2.1	34
16	Multiple Cell Upset Correction in Memories Using Difference Set Codes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 2592-2599.	3.5	32
17	Fault Tolerant Parallel Filters Based on Error Correction Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 384-387.	2.1	32
18	Low Delay Single Symbol Error Correction Codes Based on Reed Solomon Codes. IEEE Transactions on Computers, 2015, 64, 1497-1501.	2.4	30

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19	New Protection Techniques Against SEUs for Moving Average Filters in a Radiation Environment. IEEE Transactions on Nuclear Science, 2007, 54, 957-964.	1.2	28
20	An Efficient Single and Double-Adjacent Error Correcting Parallel Decoder for the (24,12) Extended Golay Code. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1603-1606.	2.1	28
21	Energy Efficiency in Industrial Ethernet: The Case of Powerlink. IEEE Transactions on Industrial Electronics, 2010, 57, 2896-2903.	5.2	27
22	Structural DMR: A Technique for Implementation of Soft-Error-Tolerant FIR Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 512-516.	2.2	27
23	Efficient error detection in Double Error Correction BCH codes for memory applications. Microelectronics Reliability, 2012, 52, 1528-1530.	0.9	26
24	Improving counting Bloom filter performance with fingerprints. Information Processing Letters, 2016, 116, 304-309.	0.4	26
25	Diverse Double Modular Redundancy: A New Direction for Soft-Error Detection and Correction. IEEE Design and Test, 2013, 30, 87-95.	1.1	24
26	Towards an energy efficient 10 Gb/s optical ethernet: Performance analysis and viability. Optical Switching and Networking, 2011, 8, 131-138.	1.2	23
27	A Class of SEC-DED-DAEC Codes Derived From Orthogonal Latin Square Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 968-972.	2.1	23
28	Parallel d-Pipeline: A Cuckoo Hashing Implementation for Increased Throughput. IEEE Transactions on Computers, 2016, 65, 326-331.	2.4	23
29	ACME: A Tool to Improve Configuration Memory Fault Injection in SRAM-Based FPGAs. IEEE Access, 2019, 7, 128153-128161.	2.6	23
30	Study of the effects of MBUs on the reliability of a 150 nm SRAM device. , 2008, , .		22
31	Characterizing a RISC-V SRAM-based FPGA implementation against Single Event Upsets using fault injection. Microelectronics Reliability, 2017, 78, 205-211.	0.9	22
32	Analysis of the Critical Bits of a RISC-V Processor Implemented in an SRAM-Based FPGA for Space Applications. Electronics (Switzerland), 2020, 9, 175.	1.8	22
33	Reliability of Single-Error Correction Protected Memories. IEEE Transactions on Reliability, 2009, 58, 193-201.	3.5	21
34	Study of the Effects of Multibit Error Correction Codes on the Reliability of Memories in the Presence of MBUs. IEEE Transactions on Device and Materials Reliability, 2009, 9, 31-39.	1.5	21
35	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 769-773.	2.1	21
36	A (64,45) Triple Error Correction Code for Memory Applications. IEEE Transactions on Device and Materials Reliability, 2012, 12, 101-106.	1.5	20

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37	Concurrent Error Detection for Orthogonal Latin Squares Encoders and Syndrome Computation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 2334-2338.	2.1	20
38	Majority Voting-Based Reduced Precision Redundancy Adders. IEEE Transactions on Device and Materials Reliability, 2018, 18, 122-124.	1.5	20
39	An ALU Protection Methodology for Soft Processors on SRAM-Based FPGAs. IEEE Transactions on Computers, 2019, 68, 1404-1410.	2.4	20
40	Evaluating the Impact of the Instruction Set on Microprocessor Reliability to Soft Errors. IEEE Transactions on Device and Materials Reliability, 2018, 18, 70-79.	1.5	19
41	An Efficient Methodology for On-Chip SEU Injection in Flip-Flops for Xilinx FPGAs. IEEE Transactions on Nuclear Science, 2018, 65, 989-996.	1.2	19
42	Efficient Protection Techniques Against SEUs for Adaptive Filters: An Echo Canceller Case Study. IEEE Transactions on Nuclear Science, 2008, 55, 1700-1707.	1.2	18
43	Increasing Reliability of FPGA-Based Adaptive Equalizers in the Presence of Single Event Upsets. IEEE Transactions on Nuclear Science, 2011, 58, 1072-1077.	1.2	17
44	Area efficient concurrent error detection and correction for parallel filters. Electronics Letters, 2012, 48, 1258.	0.5	17
45	A Simulation Platform for the Study of Soft Errors on Signal Processing Circuits through Software Fault Injection. , 2007, , .		16
46	Combined SEU and SEFI Protection for Memories Using Orthogonal Latin Square Codes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1933-1943.	3.5	16
47	Error Detection Technique for a Median Filter. IEEE Transactions on Nuclear Science, 2017, , 1-1.	1.2	16
48	Improving Memory Reliability Against Soft Errors Using Block Parity. IEEE Transactions on Nuclear Science, 2011, 58, 981-986.	1.2	15
49	A Method to Extend Orthogonal Latin Square Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1635-1639.	2.1	15
50	Efficient Protection of the Register File in Soft-Processors Implemented on Xilinx FPGAs. IEEE Transactions on Computers, 2018, 67, 299-304.	2.4	15
51	Efficient error detection codes for multiple-bit upset correction in SRAMs with BICS. ACM Transactions on Design Automation of Electronic Systems, 2009, 14, 1-10.	1.9	14
52	FastTag: A Technique to Protect Cache Tags Against Soft Errors. IEEE Transactions on Device and Materials Reliability, 2014, 14, 935-937.	1.5	14
53	Fault Tolerant Single Error Correction Encoders. Journal of Electronic Testing: Theory and Applications (JETTA), 2011, 27, 215-218.	0.9	13
54	Efficient Arithmetic-Residue-Based SEU-Tolerant FIR Filter Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 497-501.	2.2	13

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55	Comparison of the Susceptibility to Soft Errors of SRAM-Based FPGA Error Correction Codes Implementations. IEEE Transactions on Nuclear Science, 2012, 59, 619-624.	1.2	12
56	A Scheme to Improve the Intrinsic Error Detection of the Instruction Set Architecture. IEEE Computer Architecture Letters, 2017, 16, 103-106.	1.0	12
57	Optimizing Scrubbing Sequences for Advanced Computer Memories. IEEE Transactions on Device and Materials Reliability, 2010, 10, 192-200.	1.5	11
58	Efficient Soft Error-Tolerant Adaptive Equalizers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2032-2040.	3.5	11
59	Low Complexity Concurrent Error Detection for Complex Multiplication. IEEE Transactions on Computers, 2013, 62, 1899-1903.	2.4	11
60	A Comment on â€œFast Bloom Filters and Their Generalizationâ€• IEEE Transactions on Parallel and Distributed Systems, 2016, 27, 303-304.	4.0	11
61	Single Event Transient Tolerant Bloom Filter Implementations. IEEE Transactions on Computers, 2017, 66, 1831-1836.	2.4	11
62	SEFI Protection for Nanosat 16-Bit Chip Onboard Computer Memories. IEEE Transactions on Device and Materials Reliability, 2017, 17, 698-707.	1.5	11
63	A Scheme to Design Concurrent Error Detection Techniques for the Fast Fourier Transform Implemented in SRAM-Based FPGAs. IEEE Transactions on Computers, 2018, 67, 1039-1045.	2.4	11
64	Selection of the Optimal Memory Configuration in a System Affected by Soft Errors. IEEE Transactions on Device and Materials Reliability, 2009, 9, 403-411.	1.5	10
65	Improving Energy Efficiency in IEEE 802.3ba High-Rate Ethernet Optical Links. IEEE Journal of Selected Topics in Quantum Electronics, 2011, 17, 419-427.	1.9	10
66	Study of the potential energy savings in Ethernet by combining Energy Efficient Ethernet and Adaptive Link Rate. European Transactions on Telecommunications, 2012, 23, 227-233.	1.2	10
67	Low-cost single error correction multiple adjacent error correction codes. Electronics Letters, 2012, 48, 1470.	0.5	10
68	A Synergetic Use of Bloom Filters for Error Detection and Correction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 584-587.	2.1	10
69	A Method to Design Single Error Correction Codes With Fast Decoding for a Subset of Critical Bits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 171-175.	2.2	10
70	Signal shaping dual modular redundancy for soft error tolerant finite impulse response filters. Electronics Letters, 2011, 47, 1272.	0.5	9
71	Error-Detection Enhanced Decoding of Difference Set Codes for Memory Applications. IEEE Transactions on Device and Materials Reliability, 2012, 12, 335-340.	1.5	9
72	Efficient Coding Schemes for Fault-Tolerant Parallel Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 666-670.	2.2	9

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73	Performance analysis and improvements for a simulation-based fault injection platform. , 2008, , .		8
74	A fast and efficient technique to apply Selective TMR through optimization. Microelectronics Reliability, 2011, 51, 2388-2401.	0.9	8
75	Using Single Error Correction Codes to Protect Against Isolated Defects and Soft Errors. IEEE Transactions on Reliability, 2013, 62, 238-243.	3.5	8
76	A New Protection Technique for Finite Impulse Response (FIR) Filters in the Presence of Soft Errors. , 2007, , .		7
77	A technique to calculate the MBU distribution of a memory under radiation suffering the event accumulation problem. , 2008, , .		7
78	Low Power embedded DRAM caches using BCH code partitioning. , 2012, , .		7
79	Reducing the Cost of Triple Adjacent Error Correction in Double Error Correction Orthogonal Latin Square Codes. IEEE Transactions on Device and Materials Reliability, 2016, 16, 269-271.	1.5	7
80	Unequal error protection codes derived from SECâ€ÐED codes. Electronics Letters, 2016, 52, 619-620.	0.5	7
81	A Scheme to Reduce the Number of Parity Check Bits in Orthogonal Latin Square Codes. IEEE Transactions on Reliability, 2017, 66, 518-528.	3.5	7
82	Efficient Fault-Tolerant Design for Parallel Matched Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 366-370.	2.2	7
83	Radiation Hardened Digital Direct Synthesizer With CORDIC for Spaceborne Applications. IEEE Access, 2020, 8, 83167-83176.	2.6	7
84	Toward a Fault-Tolerant Star Tracker for Small Satellite Applications. IEEE Transactions on Aerospace and Electronic Systems, 2020, 56, 3421-3431.	2.6	7
85	Analyzing the impact of the Operating System on the Reliability of a RISC-V FPGA Implementation. , 2020, , .		7
86	Protection against soft errors in the space environment: A finite impulse response (FIR) filter case study. The Integration VLSI Journal, 2009, 42, 128-136.	1.3	6
87	Enhanced Implementations of Hamming Codes to Protect FIR Filters. IEEE Transactions on Nuclear Science, 2010, 57, 2112-2118.	1.2	6
88	On the Use of Euclidean Geometry Codes for Efficient Multibit Error Correction on Memory Systems. IEEE Transactions on Nuclear Science, 2012, 59, 824-828.	1.2	6
89	Reducing the Cost of Implementing Error Correction Codes in Content Addressable Memories. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 432-436.	2.2	6
90	An experimental power profile of Energy Efficient Ethernet switches. Computer Communications, 2014, 50, 110-118.	3.1	6

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91	Energy Efficient Exact Matching for Flow Identification with Cuckoo Affinity Hashing. IEEE Communications Letters, 2014, 18, 885-888.	2.5	6
92	Implementing Double Error Correction Orthogonal Latin Squares Codes in SRAM-based FPGAs. Microelectronics Reliability, 2016, 56, 221-227.	0.9	6
93	Fault tolerant encoders for Single Error Correction and Double Adjacent Error Correction codes. Microelectronics Reliability, 2018, 81, 167-173.	0.9	6
94	Reliability Analysis of the SHyLoC CCSDS123 IP Core for Lossless Hyperspectral Image Compression Using COTS FPGAs. Electronics (Switzerland), 2020, 9, 1681.	1.8	6
95	Reliability analysis of memories protected with BICS and a per-word parity bit. ACM Transactions on Design Automation of Electronic Systems, 2010, 15, 1-15.	1.9	5
96	Implementing Concurrent Error Detection in Infinite-Impulse-Response Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 583-586.	2.2	5
97	Efficient single event upset-tolerant FIR filter design based on residue number for OBP satellite communication systems. China Communications, 2013, 10, 55-67.	2.0	5
98	Exploiting processor features to implement error detection in reduced precision matrix multiplications. Microprocessors and Microsystems, 2014, 38, 581-584.	1.8	5
99	A method to protect Bloom filters from soft errors. , 2015, , .		5
100	A fault-tolerant implementation of the median filter. , 2016, , .		5
101	Unequal Error Protection Codes Derived from Double Error Correction Orthogonal Latin Square Codes. IEEE Transactions on Computers, 2016, 65, 2932-2938.	2.4	5
102	A method to recover critical bits under a double error in SEC-DED protected memories. Microelectronics Reliability, 2017, 73, 92-96.	0.9	5
103	Multiple Cell Upset Injection in BRAMs for Xilinx FPGAs. IEEE Transactions on Device and Materials Reliability, 2018, 18, 636-638.	1.5	5
104	Fault Injection Emulation for Systems in FPGAs: Tools, Techniques and Methodology, a Tutorial. Sensors, 2021, 21, 1392.	2.1	5
105	RISC-V Galois Field ISA Extension for Non-Binary Error-Correction Codes and Classical and Post-Quantum Cryptography. IEEE Transactions on Computers, 2022, , 1-1.	2.4	5
106	A macroscopic time and cost estimation model allowing task parallelism and hardware sharing for the codesign partitioning process. , 0, , .		4
107	A method to eliminate the event accumulation problem from a memory affected by multiple bit upsets. Microelectronics Reliability, 2009, 49, 707-715.	0.9	4
108	Offset DMR: A Low Overhead Soft Error Detection and Correction Technique for Transform-Based Convolution. IEEE Transactions on Computers, 2011, 60, 1511-1516.	2.4	4

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109	Reducing the Cost of Single Error Correction With Parity Sharing. IEEE Transactions on Device and Materials Reliability, 2013, 13, 420-422.	1.5	4
110	An Efficient Technique to Protect Serial Shift Registers Against Soft Errors. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 512-516.	2.2	4
111	Optimizing the Implementation of SECâ€“DAEC Codes in FPGAs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3538-3542.	2.1	4
112	Combined Modular Key and Data Error Protection for Content-Addressable Memories. IEEE Transactions on Computers, 2017, 66, 1085-1090.	2.4	4
113	A Comparison of Dual Modular Redundancy and Concurrent Error Detection in Finite Impulse Response Filters Implemented in SRAM-Based FPGAs Through Fault Injection. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 376-380.	2.2	4
114	Reducing the Power Consumption of Fault Tolerant Registers Through Hybrid Protection. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1293-1302.	3.5	4
115	Protecting Image Processing Pipelines against Configuration Memory Errors in SRAM-Based FPGAs. Electronics (Switzerland), 2018, 7, 322.	1.8	4
116	Enhancing Instruction TLB Resilience to Soft Errors. IEEE Transactions on Computers, 2018, , 1-1.	2.4	4
117	Protection Scheme for Star Tracker Images. IEEE Transactions on Aerospace and Electronic Systems, 2019, 55, 486-492.	2.6	4
118	An Experimental Analysis of SEU Sensitiveness on System Knowledge-based Hardening Techniques. , 2007, , .		3
119	A new EDAC technique against soft errors based on pulse detectors. , 2008, , .		3
120	Soft error detection and correction for FFT based convolution using different block lengths. , 2009, , .		3
121	Fault tolerant FIR filters using hamming codes. , 2009, , .		3
122	Number of Events and Time to Failure Distributions for Error Correction Protected Memories. IEEE Transactions on Device and Materials Reliability, 2010, 10, 381-389.	1.5	3
123	Mitigating the effects of large multiple cell upsets (MCUs) in memories. ACM Transactions on Design Automation of Electronic Systems, 2011, 16, 1-10.	1.9	3
124	On the expected longest length probe sequence for hashing with separate chaining. Journal of Discrete Algorithms, 2011, 9, 307-312.	0.7	3
125	Enhanced Duplication: a Technique to Correct Soft Errors in Narrow Values. IEEE Computer Architecture Letters, 2013, 12, 13-16.	1.0	3
126	Soft error tolerant Content Addressable Memories (CAMs) using error detection codes and duplication. Microprocessors and Microsystems, 2013, 37, 1103-1107.	1.8	3

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127	Verification of SRAM MСUs calculation technique for experiment time optimization. , 2013, , .		3
128	Optimized parallel decoding of difference set codes for high speed memories. Microelectronics Reliability, 2014, 54, 2645-2648.	0.9	3
129	Efficient Flow Sampling With Back-Annotated Cuckoo Hashing. IEEE Communications Letters, 2014, 18, 1695-1698.	2.5	3
130	Efficient implementation of error correction codes in hash tables. Microelectronics Reliability, 2014, 54, 338-340.	0.9	3
131	DMR+: An efficient alternative to TMR to protect registers in Xilinx FPGAs. Microelectronics Reliability, 2016, 63, 314-318.	0.9	3
132	Oddâ€weightâ€column SECâ€“DEDâ€“TAED codes. Electronics Letters, 2016, 52, 119-120.	0.5	3
133	Modular fault tolerant processor architecture on a SoC for space. Microelectronics Reliability, 2018, 83, 84-90.	0.9	3
134	An Efficient Fault-Tolerance Design for Integer Parallel Matrixâ€“Vector Multiplications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 211-215.	2.1	3
135	Enhanced Limited Magnitude Error Correcting Codes for Multilevel Cell Main Memories. IEEE Nanotechnology Magazine, 2019, 18, 1023-1026.	1.1	3
136	An Algorithmic-Based Fault Detection Technique for the 1-D Discrete Cosine Transform. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1336-1340.	2.1	3
137	Flexible and area-efficient Galois field Arithmetic Logic Unit for soft-core processors. Computers and Electrical Engineering, 2022, 99, 107759.	3.0	3
138	Optimised decoding of oddâ€weight single error correction double error detection codes with 64 bits. Electronics Letters, 2013, 49, 1617-1618.	0.5	2
139	A fault tolerant implementation of the Goertzel algorithm. Microelectronics Reliability, 2014, 54, 335-337.	0.9	2
140	A novel concurrent error detection technique for the fast Fourier transform implemented in SRAM-based FPGAs. , 2016, , .		2
141	Efficient fault tolerant parallel matrix-vector multiplications. , 2016, , .		2
142	A Methodology to Analyze the Fault Tolerance of Demosaicking Methods against Memory Single Event Functional Interrupts (SEFIs). Electronics (Switzerland), 2020, 9, 1619.	1.8	2
143	Reliability Analysis of ASIC Designs With Xilinx SRAM-Based FPGAs. IEEE Access, 2021, 9, 140676-140685.	2.6	2
144	An analysis of FPGA configuration memory SEU accumulation and a preventative scrubbing technique. Microprocessors and Microsystems, 2022, 90, 104467.	1.8	2

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145	System knowledge-based techniques against SEUs for adaptive filters. , 2007, , .		1
146	Validation and optimization of TMR protections for circuits in radiation environments. , 2011, , .		1
147	Mitigation of permanent faults in adaptive equalizers. Microelectronics Reliability, 2011, 51, 703-710.	0.9	1
148	Designing ad-hoc scrubbing sequences to improve memory reliability against soft errors. , 2011, , .		1
149	Network monitoring for energy efficiency in large-scale networks: the case of the Spanish Academic Network. Journal of Supercomputing, 2012, 62, 1284-1304.	2.4	1
150	Implementing error detection in fast counting Bloom filters. Electronics Letters, 2014, 50, 1602-1604.	0.5	1
151	Comments on â€œExtend orthogonal Latin square codes for 32-bit data protection in memory applicationsâ€•Microelectron. Reliab. 63, 278â€“283 (2016). Microelectronics Reliability, 2017, 69, 126-129.	0.9	1
152	A Fast Technique to Reduce Power Consumption on Linear Block Codes Used to Protect Registers. IEEE Transactions on Device and Materials Reliability, 2018, 18, 189-196.	1.5	1
153	Seu and Sefi error detection and correction on a ddr3 memory system. Microelectronics Reliability, 2018, 91, 23-30.	0.9	1
154	Efficient Majority-Logic Reed-Solomon Decoders for Single Symbol Correction. IEEE Transactions on Device and Materials Reliability, 2020, 20, 390-394.	1.5	1
155	Combined symbol error correction and spare through-silicon vias for 3D memories. IEEE Transactions on Emerging Topics in Computing, 2020, , 1-1.	3.2	1
156	Low delay non-binary error correction codes based on Orthogonal Latin Squares. The Integration VLSI Journal, 2021, 76, 55-60.	1.3	1
157	ACME-2: Improving the Extraction of Essential Bits in Xilinx SRAM-Based FPGAs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1577-1581.	2.2	1
158	Reduction of Parity Overhead in a Subset of Orthogonal Latin Square Codes. , 2020, , .		1
159	A grouping partitioning technique with automatic criterion selection for the codesign process. , 0, , .		0
160	The heterogeneous structure problem in hardware/software codesign: a macroscopic approach. , 0, , .		0
161	New Alternatives to the Estimation Problem in Hardware-Software Codesign of Complex Embedded Systems: The H.261 Video Co-dec Case Study. Design Automation for Embedded Systems, 2004, 9, 193-210.	0.7	0
162	Fault Tolerance Analysis of Communication System Interleavers: the 802.11a Case Study. Journal of Signal Processing Systems, 2008, 52, 231-247.	1.4	0

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163	Selection of the optimal interleaving distance for memories suffering MCUs. , 2009, , .		0
164	Very-low-complexity concurrent error detection for transform-based filters. Electronics Letters, 2010, 46, 1677.	0.5	0
165	Low-complexity Concurrent Error Detection for convolution with Fast Fourier Transforms. Microelectronics Reliability, 2011, 51, 1152-1156.	0.9	0
166	Efficient error detection in multiple way tables. Electronics Letters, 2015, 51, 50-52.	0.5	0
167	Efficient implementation of single event upset tolerant register comparison. Electronics Letters, 2016, 52, 1922-1923.	0.5	0
168	A method to protect Cuckoo filters from soft errors. Microelectronics Reliability, 2017, 72, 85-89.	0.9	0
169	Low-Latency and Low-Power Test-Vector Selector for Reed-Solomonâ€™s Low-Complexity Chase. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3362-3366.	2.2	0
170	Decoding Algorithm for Quadruple-Error-Correcting Reed-Solomon Codes and Its Derived Architectures. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1438-1442.	2.2	0
171	Energy Efficiency in Ethernet. , 0, , 277-290.		0
172	A new radiation-hardened architecture for holographic memory address calculation. AEJ - Alexandria Engineering Journal, 2022, 61, 6181-6190.	3.4	0