S D Cotofana

List of Publications by Year
in descending order

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143 papers	1,964 citations	516710 16 h-index	361022 35 g-index
177 all docs	177 docs citations	177 times ranked	1062 citing authors

#	Article	IF	Citations
1	A Spin Wave-Based Approximate 4:2 Compressor: Seeking the most energy-efficient digital computing paradigm. IEEE Nanotechnology Magazine, 2022, 16, 47-56.	1.3	2
2	Advances in Magnetics Roadmap on Spin-Wave Computing. IEEE Transactions on Magnetics, 2022, 58, 1-72.	2.1	179
3	Would Magnonic Circuits Outperform CMOS Counterparts?. , 2022, , .		1
4	Non-Binary Spin Wave Based Circuit Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 3888-3900.	5.4	1
5	Efficient Computation Reduction in Bayesian Neural Networks Through Feature Decomposition and Memorization. IEEE Transactions on Neural Networks and Learning Systems, 2021, 32, 1703-1712.	11.3	17
6	Spin Wave Normalization Toward All Magnonic Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 536-549.	5.4	14
7	A Reconfigurable Graphene-Based Spiking Neural Network Architecture. IEEE Open Journal of Nanotechnology, 2021, 2, 59-71.	2.0	4
8	Fan-out of 2 Triangle Shape Spin Wave Logic Gates. , 2021, , .		3
9	Achieving Wave Pipelining in Spin Wave Technology. , 2021, , .		4
10	Multifrequency Data Parallel Spin Wave Logic Gates. IEEE Transactions on Magnetics, 2021, 57, 1-12.	2.1	8
11	Spin Wave Based Full Adder. , 2021, , .		6
12	Graphene-Based Artificial Synapses with Tunable Plasticity. ACM Journal on Emerging Technologies in Computing Systems, 2021, 17, 1-21.	2.3	4
13	The 2021 Magnonics Roadmap. Journal of Physics Condensed Matter, 2021, 33, 413001.	1.8	287
14	Spin Wave Based 4-2 Compressor. , 2021, , .		1
15	Reliability Aware Design and Lifetime Management of Computing Platforms. IEEE Transactions on Emerging Topics in Computing, 2020, 8, 602-615.	4.6	0
16	A magnonic directional coupler for integrated magnonic half-adders. Nature Electronics, 2020, 3, 765-774.	26.0	139
17	2-Output Spin Wave Programmable Logic Gate. , 2020, , .		9
18	Ultra-Compact, Entirely Graphene-Based Nonlinear Leaky Integrate-and-Fire Spiking Neuron. , 2020, , .		6

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19	Introduction to spin wave computing. Journal of Applied Physics, 2020, 128, .	2.5	179
20	A Self-Matching Complementary-Reference Sensing Scheme for High-Speed and Reliable Toggle Spin Torque MRAM. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4247-4258.	5.4	23
21	Compact Graphene-Based Spiking Neural Network With Unsupervised Learning Capabilities. IEEE Open Journal of Nanotechnology, 2020, 1, 135-144.	2.0	6
22	Fan-out enabled spin wave majority gate. AIP Advances, 2020, 10, .	1.3	24
23	n-bit Data Parallel Spin Wave Logic Gate. , 2020, , .		11
24	4-output Programmable Spin Wave Logic Gate. , 2020, , .		2
25	NBTI stress delay sensitivity analysis of reliability enhanced Schmitt trigger based circuits. Microelectronics Reliability, 2019, 102, 113391.	1.7	3
26	Atomistic-Level Hysteresis-Aware Graphene Structures Electron Transport Model. , 2019, , .		8
27	Graphene Nanoribbon Based Complementary Logic Gates and Circuits. IEEE Nanotechnology Magazine, 2019, 18, 287-298.	2.0	34
28	On Basic Boolean Function Graphene Nanoribbon Conductance Mapping. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1948-1959.	5.4	10
29	Low-Leakage 3D Stacked Hybrid NEMFET-CMOS DualÂPort Memory. IEEE Transactions on Emerging Topics in Computing, 2018, 6, 184-199.	4.6	5
30	Complementary Arranged Graphene Nanoribbon-based Boolean Gates. , 2018, , .		6
31	On Carving Basic Boolean Functions on Graphene Nanoribbons Conduction Maps. , 2018, , .		8
32	Towards Maximum Utilization of Remained Bandwidth in Defected NoC Links. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 285-298.	2.7	4
33	A Mixed-Size Monolithic 3D Placer with 2D Layout Inheritance. , 2017, , .		4
34	High-Performance, Cost-Effective 3D Stacked Wide-Operand Adders. IEEE Transactions on Emerging Topics in Computing, 2017, 5, 179-192.	4.6	1
35	LDPC-Based Adaptive Multi-Error Correction for 3D Memories. , 2017, , .		0
36	Low cost multi-error correction for 3D polyhedral memories. , 2017, , .		1

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37	An approach for digital Circuit Error/Reliability Propagation Analysis based on Conditional Probability. , 2016, , .		0
38	Ultraâ€low leakage SRAM design with subâ€32Ânm tunnel FETs for low standby power applications. Micro and Nano Letters, 2016, 11, 828-831.	1.3	5
39	Flexible, Cost-Efficient, High-Throughput Architecture for Layered LDPC Decoders with Fully-Parallel Processing Units. , 2016, , .		19
40	Multi-level probabilistic timing error reliability analysis using a circuit dependent fault map generation. , 2015, , .		0
41	Timing error analysis of flooded LDPC decoders. , 2015, , .		5
42	ROST-C: Reliability driven optimisation and synthesis techniques for combinational circuits. , 2015, , .		2
43	Inverse Gaussian distribution based timing analysis of Sub-threshold CMOS circuits. Microelectronics Reliability, 2015, 55, 2754-2761.	1.7	7
44	A shared polyhedral cache for 3D wide-I/O multi-core computing platforms. , 2015, , .		2
45	Asynchronous Charge Sharing Power Consistent Montgomery Multiplier. , 2015, , .		0
46	Dynamic Bitstream Length Scaling Energy Effective Stochastic LDPC Decoding. , 2015, , .		0
47	Transmission Channel Noise Aware Energy Effective LDPC Decoding. IFIP Advances in Information and Communication Technology, 2015, , 198-219.	0.7	1
48	Link Bandwidth Aware Backtracking Based Dynamic Task Mapping in NoC based MPSoCs. , 2014, , .		4
49	EFFICIENT METHOD FOR DESIGNING MODULO {2n Â± k} MULTIPLIERS. Journal of Circuits, Systems and Computers, 2014, 23, 1450001.	1.5	7
50	Towards energy effective LDPC decoding by exploiting channel noise variability. , 2014, , .		2
51	Energy effective 3D stacked hybrid NEMFET-CMOS caches. , 2014, , .		1
52	Robust sub-powered asynchronous logic. , 2014, , .		2
53	An efficient residue-to-binary converter for the new moduli set {2^{n/2} ± 1, 2²ⁿ⁺¹,2ⁿ + 1}. , 2014, , .		0
54	Analysis of the impact of spatial and temporal variations on the stability of SRAM arrays and the mitigation technique using independent-gate devices. Journal of Parallel and Distributed Computing, 2014, 74, 2521-2529.	4.1	7

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55	Linear Compositional Delay Model for the Timing Analysis of Sub-Powered Combinational Circuits. , 2014, , .		11
56	Energy effective 3D stacked hybrid NEMFET-CMOS caches. , 2014, , .		1
57	A nonlinear degradation path dependent end-of-life estimation framework from noisy observations. Microelectronics Reliability, 2013, 53, 1213-1217.	1.7	11
58	Controlled Degradation Stochastic Resonance in Adaptive Averaging Cell-Based Architectures. IEEE Nanotechnology Magazine, 2013, 12, 888-896.	2.0	2
59	Ultra low power NEMFET based logic. , 2013, , .		10
60	Embedded computer architecture laboratory. , 2013, , .		4
61	An effective New CRT based reverse converter for a novel moduli set {2²ⁿ⁺¹ − 1, 2²ⁿ⁺¹, 2²ⁿ − 1}. , 2013, , .		2
62	VASILE: A reconfigurable vector architecture for instruction level frequency scaling. , 2013, , .		2
63	Stigmergic search with single electron tunneling technology based memory enhanced hubs. , 2012, , .		5
64	A Markovian, variation-aware circuit-level aging model. , 2012, , .		1
65	Decoupled inter- and intra-application scheduling for composable and robust embedded MPSoC platforms. , 2012, , .		10
66	Adaptive Fault-Tolerant Architecture for Unreliable Technologies With Heterogeneous Variability. IEEE Nanotechnology Magazine, 2012, 11, 818-829.	2.0	4
67	Is 3D integration the way to future dependable computing platforms?. , 2012, , .		6
68	Degradation Stochastic Resonance (DSR) in AD-AVG architectures. , 2012, , .		3
69	Variation tolerant on-chip degradation sensors for dynamic reliability management systems. Microelectronics Reliability, 2012, 52, 1787-1791.	1.7	21
70	Adaptive fault-tolerant architecture for unreliable device technologies. , 2011, , .		1
71	Towards “zero-energy” using NEMFET-based power management for 3D hybrid stacked ICs. , 2011, , .		6
72	An Efficient FPGA Design of Residue-to-Binary Converter for the Moduli Set ${2n+1,2n,2n-1}$. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1500-1503.	3.1	14

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73	A unified aging model of NBTI and HCI degradation towards lifetime reliability management for nanoscale MOSFET circuits. , 2011, , .		37
74	Composable local memory organisation for streaming applications on embedded MPSoCs. , 2011, , .		5
75	Functional unit sharing between stacked processors in 3D integrated systems. , 2011, , .		3
76	An improved RNS reverse converter for the {2²ⁿ⁺¹−1, 2ⁿ, 2ⁿ−1} moduli set. , 2010, , .		11
77	Single Electron Tunneling based computation. , 2010, , .		1
78	Memoryless RNS-to-binary converters for the {2ⁿ⁺¹ - 1, 2ⁿ, 2ⁿ - 1} moduli set. , 2010, , .		3
79	A master equation model of multi-island single-electron transistors based on stability diagram. , 2010, , .		1
80	A novel virtual age reliability model for Time-to-Failure prediction. , 2010, , .		5
81	A composable, energy-managed, real-time MPSOC platform. , 2010, , .		14
82	Advanced NEMS-based power management for 3D Stacked Integrated Circuits. , 2010, , .		3
83	Residue-to-decimal converters for moduli sets with common factors. , 2009, , .		1
84	An O(n) Residue Number System to Mixed Radix Conversion technique. , 2009, , .		15
85	Emerging non-CMOS nanoelectronic devices - What are they?. , 2009, , .		4
86	Suspended Gate Field Effect Transistor based power management - a 32-bit adder case study. , 2009, , .		0
87	Adaptive Clock Scheduling for pipelined structures. , 2009, , .		1
88	A reverse converter for the new 4-moduli set {2n + 3, 2n + 2, 2n + 1, 2n}. , 2009, , .		1
89	Generalized matrix method for efficient residue to decimal conversion. , 2008, , .		2
90	GRAAL: A Framework for Low-Power 3D Graphics Accelerators. IEEE Computer Graphics and Applications, 2008, 28, 63-73.	1.2	7

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91	An Analysis of Internal Parameter Variations Effects on Nanoscaled Gates. IEEE Nanotechnology Magazine, 2008, 7, 24-33.	2.0	23
92	Building Blocks for Fluctuation Based Calculation in Single Electron Tunneling Technology. , 2008, , .		5
93	Casta DIVA - a design for variability platform. , 2008, , .		2
94	A residue to binary converter for the {2n + 2, 2n + 1, 2n} moduli set. , 2008, , .		6
95	Single Electron Tunneling Delay Insensitive and fluctuation based computation paradigms and circuits. , 2008, , .		1
96	Residue Number System operands to decimal conversion for 3-moduli sets. , 2008, , .		10
97	Manufacturability Issues of Redundant Nanogates. Semiconductor Conference, 2009 CAS 2009 International, 2007, , .	0.0	0
98	Computing Division Using Single-Electron Tunneling Technology. IEEE Nanotechnology Magazine, 2007, 6, 451-459.	2.0	10
99	A Taxonomy of Field-Programmable Custom Computing Machines. , 2007, , 299-378.		0
100	Basic Building Blocks for Effective Single Electron Tunneling Technology Based Computation. , 2006, , .		1
101	Static cache partitioning robustness analysis for embedded on-chip multi-processors. , 2006, , .		4
102	Evaluation Methodology for Single Electron Encoded Threshold Logic Gates. , 2006, , 247-262.		4
103	High-Radix Addition and Multiplication in the Electron Counting Paradigm Using Single Electron Tunneling Technology. Lecture Notes in Computer Science, 2006, , 447-456.	1.3	0
104	Addition related arithmetic operations via controlled transport of charge. IEEE Transactions on Computers, 2005, 54, 243-256.	3.4	45
105	Hierarchical Testability Assisted Intelligent Simulation. International Journal of Modelling and Simulation, 2004, 24, 26-36.	3.3	0
106	Single Electron Encoded Latches and Flip-Flops. IEEE Nanotechnology Magazine, 2004, 3, 237-248.	2.0	56
107	Microcode processing: Positioning and directions. IEEE Micro, 2003, 23, 21-30.	1.8	16
108	CMOS Implementation of Generalized Threshold Functions. Lecture Notes in Computer Science, 2003, , 65-72.	1.3	3

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109	FSM non-minimal state encoding for low power. , 2002, , .		2
110	Field-Programmable Custom Computing Machines - A Taxonomy -. Lecture Notes in Computer Science, 2002, , 79-88.	1.3	16
111	The MOLEN Ïï¼4-Coded Processor. Lecture Notes in Computer Science, 2001, , 275-285.	1.3	52
112	Signed digit addition and related operations with threshold logic. IEEE Transactions on Computers, 2000, 49, 193-207.	3.4	9
113	Serial binary multiplication with feed-forward neural networks. Neurocomputing, 1999, 28, 1-19.	5.9	2
114	Periodic symmetric functions, serial addition, and multiplication with neural networks. IEEE Transactions on Neural Networks, 1998, 9, 1118-1128.	4.2	24
115	2-1 addition and related arithmetic operations with threshold logic. IEEE Transactions on Computers, 1996, 45, 1062-1067.	3.4	30
116	Î´-Bit serial binary addition with linear threshold networks. Journal of Signal Processing Systems, 1996, 14, 249-264.	1.0	4
117	Serial binary addition with polynormally bounded weights. Lecture Notes in Computer Science, 1996, , 741-746.	1.3	0
118	A low-power threshold logic family. , 0, , .		12
119	Block save addition with threshold logic. , 0, , .		2
120	On the design complexity of the issue logic of superscalar machines. , 0, , .		3
121	Counter based superscalar instruction issuing. , 0, , .		2
122	General-purpose processor Huffman encoding extension. , 0, , .		6
123	MPEG macroblock parsing and pel reconstruction on an FPGA-augmented TriMedia processor. , 0, , .		10
124	Achieving fanout capabilities in single electron encoded logic networks. , 0, , .		9
125	Coarse reconfigurable multimedia unit extension. , 0, , .		7
126	Digital to analog conversion performed in single electron technology. , 0, , .		10

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127	A linear threshold gate implementation in single electron technology. , 0, , .		74
128	Static buffered SET based logic gates. , 0, , .		31
129	High-speed hybrid threshold-Boolean logic counters and compressors. , 0, , .		6
130	MPEG-compliant entropy decoding on FPGA-augmented TriMedia/CPU64. , 0, , .		7
131	A sum of absolute differences implementation in FPGA hardware. , 0, , .		54
132	Alternatives in FPGA-based SAD implementations. , 0, , .		15
133	A full adder implementation using SET based linear threshold gates. , 0, , .		17
134	A Hierarchical sparse matrix storage format for vector processors. , 0, , .		13
135	Color space conversion for MPEG decoding on FPGA-augmented TriMedia processor. , 0, , .		6
136	Design and experimental results of a CMOS flip-flop featuring embedded threshold logic. , 0, , .		4
137	On computing addition related arithmetic operations via controlled transport of charge. , 0, , .		8
138	Single electron encoded logic memory elements. , 0, , .		2
139	Logical effort based design exploration of 64-bit adders using a mixed dynamic-CMOS/threshold-logic approach. , 0, , .		4
140	Binary addition based on single electron tunneling devices. , 0, , .		12
141	Design methodology for single electron based building blocks. , 0, , .		4
142	High Radix Addition Via Conditional Charge Transport in Single Electron Tunneling Technology. , 0, , .		3
143	Buffer design trade-offs for single electron logic gates. , 0, , .		4