Sandeep Chandran

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/1010116/publications.pdf

Version: 2024-02-01

8	20	2682572 2	2550090 3
papers	citations	h-index	g-index

8	8	8	20
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	DHOOM. , 2019, , .		4
2	Debug Data Reduction Techniques. , 2019, , 211-229.		0
3	Managing Trace Summaries to Minimize Stalls During Postsilicon Validation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1881-1894.	3.1	8
4	A Generic Implementation of Barriers Using Optical Interconnects. , 2016, , .		2
5	Extending trace history through tapered summaries in post-silicon validation. , 2016, , .		1
6	Area-Aware Cache Update Trackers for Postsilicon Validation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1794-1807.	3.1	1
7	Architectural Support for Handling Jitterin Shared Memory Based Parallel Applications. IEEE Transactions on Parallel and Distributed Systems, 2014, 25, 1166-1176.	5.6	4
8	Space Sensitive Cache Dumping for Post-silicon Validation. , 2013, , .		0