Te-Kuang Chiang

List of Publications by Year
in descending order

32 papers	562 citations	840776 11 h-index	610901 24 g-index
32 all docs	32 docs citations	32 times ranked	408 citing authors

#	Article	IF	Citations
1	A Quasi-Two-Dimensional Threshold Voltage Model for Short-Channel Junctionless Double-Gate MOSFETs. IEEE Transactions on Electron Devices, 2012, 59, 2284-2289.	3.0	135
2	A Compact Model for Threshold Voltage of Surrounding-Gate MOSFETs With Localized Interface Trapped Charges. IEEE Transactions on Electron Devices, 2011, 58, 567-571.	3.0	81
3	A New Quasi-2-D Threshold Voltage Model for Short-Channel Junctionless Cylindrical Surrounding Gate (JLCSG) MOSFETs. IEEE Transactions on Electron Devices, 2012, 59, 3127-3129.	3.0	72
4	Effects of Electrodes on the Switching Behavior of Strontium Titanate Nickelate Resistive Random Access Memory. Materials, 2015, 8, 7191-7198.	2.9	43
5	A Novel Scaling Theory for Fully Depleted, Multiple-Gate MOSFET, Including Effective Number of Gates (ENGs). IEEE Transactions on Electron Devices, 2014, 61, 631-633.	3.0	32
6	A Novel Quasi-3-D Threshold Voltage Model for Fully Depleted Quadruple-Gate (FDQG) MOSFETs: With Equivalent Number of Gates (ENG) Included. IEEE Nanotechnology Magazine, 2013, 12, 1022-1025.	2.0	25
7	A New Analytical Subthreshold Potential/Current Model for Quadruple-Gate Junctionless MOSFETs. IEEE Transactions on Electron Devices, 2014, 61, 1972-1978.	3.0	21
8	A Short-Channel-Effect-Degraded Noise Margin Model for Junctionless Double-Gate MOSFET Working on Subthreshold CMOS Logic Gates. IEEE Transactions on Electron Devices, 2016, 63, 3354-3359.	3.0	19
9	A Quasi-3-D Scaling Length Model for Trapezoidal FinFET and Its Application to Subthreshold Behavior Analysis. IEEE Nanotechnology Magazine, 2017, 16, 281-289.	2.0	15
10	A New Threshold Voltage Model for Short-Channel Junctionless Inverted T-Shaped Gate FETs (JLITFET). IEEE Nanotechnology Magazine, 2016, 15, 442-447.	2.0	14
11	A New Subthreshold Current Model for Junctionless Trigate MOSFETs to Examine Interface-Trapped Charge Effects. IEEE Transactions on Electron Devices, 2015, 62, 2745-2750.	3.0	13
12	An analytical subthreshold current/swing model for junctionless cylindrical nanowire FETs (JLCNFETs). Facta Universitatis - Series Electronics and Energetics, 2013, 26, 157-173.	0.9	13
13	A Novel Scaling Theory for Fully Depleted Omega-Gate MOSFETs Included With Equivalent Number of Gates. IEEE Transactions on Electron Devices, 2014, 61, 926-929.	3.0	10
14	Effects of Ni in Strontium Titanate Nickelate Thin Films for Flexible Nonvolatile Memory Applications. IEEE Transactions on Electron Devices, 2017, 64, 2001-2007.	3.0	10
15	A New Device-Physics-Based Noise Margin/Logic Swing Model of Surrounding-Gate MOSFET Working on Subthreshold Logic Gate. IEEE Transactions on Electron Devices, 2016, 63, 4209-4217.	3.0	7
16	A New Device-Parameter-Oriented DC Power Model for Symmetric Operation of Junctionless Double-Gate <sc> mosfet</sc> Working on Low-Power CMOS Subthreshold Logic Gates. IEEE Nanotechnology Magazine, 2018, 17, 424-431.	2.0	7
17	A New Effective-Conducting-Path-Driven Subthreshold Behavior Model for Junctionless Dual-Material Omega-Gate Nano-MOSFETs. IEEE Nanotechnology Magazine, 2019, 18, 904-910.	2.0	6
18	A Compact Interface-Trapped-Charge-Induced Subthreshold Current Model for Surrounding-Gate MOSFETs. IEEE Transactions on Device and Materials Reliability, 2014, 14, 766-768.	2.0	5

#	Article	IF	Citations
19	A Novel Quasi-3D Interface-Trapped-Charge-Degraded Threshold Voltage Model for Omega-Gate <inline-formula> <tex-math notation="TeX">$(Omega{G})$</tex-math></inline-formula> MOSFETs. IEEE Transactions on Device and Materials Reliability, 2015, 15, 35-39.	2.0	5
20	A New Quasi-3-D Compact Threshold Voltage Model for Pi-Gate (ÎG) MOSFETs With the Interface Trapped Charges. IEEE Nanotechnology Magazine, 2015, 14, 555-560.	2.0	4
21	Comparative investigation of GaAsSb/InGaAs type-II and InP/InGaAs type-I doped-channel field-effect transistors. Semiconductors, 2015, 49, 254-258.	0.5	4
22	Nanosheet FET: A new subthreshold current model caused by interface-trapped-charge and its application for evaluation of subthreshold logic gate. Microelectronics Journal, 2020, 104, 104893.	2.0	4
23	A Unified Quasi-3D Subthreshold Behavior Model for Multiple-Gate MOSFETs. IEEE Nanotechnology Magazine, 2018, , 1-1.	2.0	3
24	Junctionless Multiple-Gate (JLMG) MOSFETs: A Unified Subthreshold Current Model to Assess Noise Margin of Subthreshold Logic Gate. IEEE Transactions on Electron Devices, 2021, 68, 5330-5334.	3.0	3
25	Comparative investigation of InGaP/GaAs/GaAsBi and InGaP/GaAs heterojunction bipolar transistors. Semiconductors, 2015, 49, 1361-1364.	0.5	2
26	A novel scaling theory for fully depleted pi-gate (ÎG) MOSFETs. Solid-State Electronics, 2015, 103, 199-201.	1.4	2
27	A New Short-Channel-Effect-Degraded Subthrehold Behavior Model for Double-Fin Multi-Channel FETs (DFMcFETs). IEEE Nanotechnology Magazine, 2016, , 1-1.	2.0	2
28	A Novel Localized-Trapped-Charge-Induced Threshold Voltage Model for Double-Fin Multi-Channel FETs (DFMcFETs). IEEE Transactions on Device and Materials Reliability, 2017, 17, 291-297.	2.0	2
29	A Novel Effective-Conducting-Path-Induced Scaling Length Model and Its Application for Assessing Short-Channel Performance of Multiple-Gate MOSFETs. IEEE Transactions on Electron Devices, 2018, 65, 4535-4541.	3.0	2
30	A quasi-2D threshold voltage model for short-channel junctionless (JL) double-gate MOSFETs. , 2012, , .		1
31	Elliptical nanowire FET: Modeling the short-channel subthreshold current caused by interface-trapped-charge and its evaluation for subthreshold logic gate. Superlattices and Microstructures, 2021, 149, 106751.	3.1	0
32	Novel Omega-Gate heterojunction tunneling FET with a new analytical model. Semiconductor Science and Technology, 2021, 36, 065011.	2.0	0