Anand Raghunathan

List of Publications by Year in Descending Order

201 papers	6,108 citations	39 h-index	71 g-index
230 ext. papers	7,637 ext. citations	2.8 avg, IF	6.16 L-index

#	Paper	IF	Citations
201	Ax-BxP: Approximate Blocked Computation for Precision-reconfigurable Deep Neural Network Acceleration. *ACM Transactions on Design Automation of Electronic Systems*, **2022**, 27, 1-20	1.5	
200	Accelerating DNN Training Through Selective Localized Learning.. *Frontiers in Neuroscience*, **2021**, 15, 759807	5.1	
199	TxSim: Modeling Training of Deep Neural Networks on Resistive Crossbar Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 730-738	2.6	3
198	Probabilistic Spike Propagation for Efficient Hardware Implementation of Spiking Neural Networks. *Frontiers in Neuroscience*, **2021**, 15, 694402	5.1	1
197	RxNN: A Framework for Evaluating Deep Neural Networks on Resistive Crossbars. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 326-338	2.5	26
196	PIM-DRAM: Accelerating Machine Learning Workloads Using Processing in Commodity DRAM. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2021**, 11, 701-710	5.2	0
195	Sparsity Turns Adversarial: Energy and Latency Attacks on Deep Neural Networks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 4129-4141	2.5	2
194	Pruning Filters while Training for Efficiently Optimizing Deep Learning Networks **2020**,		6
193	Approximate Memory Compression. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* , **2020**, 28, 980-991	2.6	3
192	Valley-Coupled-Spintronic Non-Volatile Memories With Compute-In-Memory Support. *IEEE Nanotechnology Magazine*, **2020**, 19, 635-647	2.6	5
191	TiM-DNN: Ternary In-Memory Accelerator for Deep Neural Networks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 1567-1577	2.6	5
190	D y VED eep. *Transactions on Embedded Computing Systems*, **2020**, 19, 1-24	1.8	0
189	CxDNN. *Transactions on Embedded Computing Systems*, **2020**, 18, 1-23	1.8	17
188	Resistive Crossbars as Approximate Hardware Building Blocks for Machine Learning: Opportunities and Challenges. *Proceedings of the IEEE*, **2020**, 108, 2276-2310	14.3	18
187	Gradual Channel Pruning While Training Using Feature Relevance Scores for Convolutional Neural Networks. *IEEE Access*, **2020**, 8, 171924-171932	3.5	9
186	Logic Synthesis of Approximate Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 2503-2515	2.5	8
185	**2019**,		7

184	Non-Volatile Memory utilizing Reconfigurable Ferroelectric Transistors to enable Differential Read and Energy-Efficient In-Memory Computation **2019**,		5
183	. *IEEE Transactions on Magnetics*, **2019**, 55, 1-9	2	3
182	Pack and Detect **2019**,		3
181	**2019**,		2
180	X-MANN **2019**,		11
179	Manna **2019**,		9
178	SparCE: Sparsity Aware General-Purpose Core Extensions to Accelerate Deep Neural Networks. *IEEE Transactions on Computers*, **2019**, 68, 912-925	2.5	10
177	Automatic Synthesis Techniques for Approximate Circuits **2019**, 123-140		1
176	Computing in Memory With Spin-Transfer Torque Magnetic RAM. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 470-483	2.6	123
175	Computing-in-memory with spintronics **2018**,		3
174	Approximate Computing for Long Short Term Memory (LSTM) Neural Networks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 2266-2276	2.5	14
173	. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2018**, 8, 379-390	5.2	3
172	Energy-Efficient Neural Computing with Approximate Multipliers. *ACM Journal on Emerging Technologies in Computing Systems*, **2018**, 14, 1-23	1.7	27
171	SYNCVIBE: Fast and Secure Device Pairing through Physical Vibration on Commodity Smartphones **2018**,		6
170	AxBA **2018**,		11
169	. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2018**, 8, 796-809	5.2	23
168	Model-based Iterative CT Image Reconstruction on GPUs **2017**,		11
167	Wearable Medical Sensor-Based System Design: A Survey. *IEEE Transactions on Multi-Scale Computing Systems*, **2017**, 3, 124-138		69

166	Approximate computing for spiking neural networks **2017**,		19
165	A Pathway to Enable Exponential Scaling for the Beyond-CMOS Era **2017**,		14
164	Energy-Efficient Object Detection Using Semantic Decomposition. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2673-2677	2.6	3
163	Approximate Error Detection With Stochastic Checkers. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2258-2270	2.6	3
162	Yield, Area, and Energy Optimization in STT-MRAMs Using Failure-Aware ECC. *ACM Journal on Emerging Technologies in Computing Systems*, **2017**, 13, 1-20	1.7	5
161	ScaleDeep. *Computer Architecture News*, **2017**, 45, 13-26		19
160	**2017**,		10
159	Model-based Iterative CT Image Reconstruction on GPUs. *ACM SIGPLAN Notices*, **2017**, 52, 207-220	0.2	6
158	ScaleDeep **2017**,		81
157	**2017**,		18
156	DISASTER: Dedicated Intelligent Security Attacks on Sensor-Triggered Emergency Responses. *IEEE Transactions on Multi-Scale Computing Systems*, **2017**, 3, 255-268		7
155	CABA: Continuous Authentication Based on BioAura. *IEEE Transactions on Computers*, **2017**, 66, 759-772	2.5	34
154	Design and Management of Battery-Supercapacitor Hybrid Electrical Energy Storage Systems for Regulation Services. *IEEE Transactions on Multi-Scale Computing Systems*, **2017**, 3, 12-24		47
153	Asymmetric Underlapped FinFETs for Near- and Super-Threshold Logic at Sub-10nm Technology Nodes. *ACM Journal on Emerging Technologies in Computing Systems*, **2017**, 13, 1-22	1.7	1
152	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 462-475	2.6	14
151	A Programmable Event-driven Architecture for Evaluating Spiking Neural Networks **2017**,		11
150	**2017**,		14
149	Integrated Systems in the More-Than-Moore Era: Designing Low-Cost Energy-Efficient Systems Using Heterogeneous Components. *IEEE Design and Test*, **2016**, 33, 56-65	1.4	15

148	Designing approximate circuits using clock overgating **2016**,		14
147	Invited - Cross-layer approximations for neuromorphic computing: from devices to circuits and systems **2016**,		22
146	Neuromorphic Computing Enabled by Spin-Transfer Torque Devices **2016**,		1
145	. *Proceedings of the IEEE*, **2016**, 104, 1449-1488	14.3	97
144	Emulation-Based Analysis of System-on-Chip Performance Under Variations. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 3401-3414	2.6	0
143	Asymmetric Underlapped Sub-10-nm n-FinFETs for High-Speed and Low-Leakage 6T SRAMs. *IEEE Transactions on Electron Devices*, **2016**, 63, 1034-1040	2.9	9
142	. *IEEE Transactions on Computers*, **2016**, 65, 1010-1024	2.5	19
141	Efficient embedded learning for IoT devices **2016**,		10
140	High performance model based image reconstruction **2016**,		12
139	Embedding Read-Only Memory in Spin-Transfer Torque MRAM-Based On-Chip Caches. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 992-1002	2.6	8
138	Physiological Information Leakage: A New Frontier in Health Information Security. *IEEE Transactions on Emerging Topics in Computing*, **2016**, 4, 321-334	4.1	23
137	Spin-Transfer Torque Devices for Logic and Memory: Prospects and Perspectives. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 1-22	2.5	114
136	**2016**,		2
135	Multiplier-less Artificial Neurons exploiting error resiliency for energy-efficient neural computing **2016**,		7
134	EMBIRA: An Accelerator for Model-Based Iterative Reconstruction. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 3243-3256	2.6	
133	Reliability and security of implantable and wearable medical devices **2015**, 167-199		3
132	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 1017-1030	2.6	11
131	Approximate computing and the quest for computing efficiency **2015**,		125

130	Approximate storage for energy efficient spintronic memories **2015**,		47
129	Vibration-based secure side channel for medical devices **2015**,		24
128	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 1441-1454	2.5	13
127	Energy-Efficient All-Spin Cache Hierarchy Using Shift-Based Writes and Multilevel Storage. *ACM Journal on Emerging Technologies in Computing Systems*, **2015**, 12, 1-27	1.7	3
126	Scalable-effort classifiers for energy-efficient machine learning **2015**,		39
125	Approximate Computing: An Energy-Efficient Computing Technique for Error Resilient Applications **2015**,		22
124	Systematic Poisoning Attacks on and Defenses for Machine Learning in Healthcare. *IEEE Journal of Biomedical and Health Informatics*, **2015**, 19, 1893-905	7.2	85
123	Quality Configurable Reduce-and-Rank for Energy Efficient Approximate Computing **2015**,		12
122	Computing Approximately, and Efficiently **2015**,		15
121	Asymmetric underlapped FinFET based robust SRAM design at 7nm node **2015**,		5
120	DyReCTape: A dynamically reconfigurable cache using domain wall memory tapes **2015**,		8
119	Spintastic: Spin-based stochastic logic for energy-efficient computing **2015**,		20
118	Energy-Efficient Long-term Continuous Personal Health Monitoring. *IEEE Transactions on Multi-Scale Computing Systems*, **2015**, 1, 85-98		62
117	STT-SNN: A Spin-Transfer-Torque Based Soft-Limiting Non-Linear Neuron for Low-Power Artificial Neural Networks. *IEEE Nanotechnology Magazine*, **2015**, 14, 1013-1023	2.6	37
116	An Application Adaptation Approach to Mitigate the Impact of Dynamic Thermal Management on Video Encoding. *ACM Transactions on Design Automation of Electronic Systems*, **2015**, 20, 1-27	1.5	1
115	Domain-Specific Many-core Computing using Spin-based Memory. *IEEE Nanotechnology Magazine*, **2014**, 13, 881-894	2.6	6
114	ASLAN: Synthesis of approximate sequential circuits **2014**,		14
113	STAG: Spintronic-Tape Architecture for GPGPU cache hierarchies **2014**,		11

112	A defense framework against malware and vulnerability exploits. *International Journal of Information Security*, **2014**, 13, 439-452	2.8	8
111	STAG. *Computer Architecture News*, **2014**, 42, 253-264		24
110	AxNN **2014**,		134
109	Trustworthiness of Medical Devices and Body Area Networks. *Proceedings of the IEEE*, **2014**, 102, 1174-1188		71
108	Variation Aware Cache Partitioning for Multithreaded Programs **2014**,		3
107	SPINDLE **2014**,		54
106	Variation tolerant design of a vector processor for recognition, mining and synthesis **2014**,		3
105	StoRM **2014**,		19
104	Non-Volatile Complementary Polarizer Spin-Transfer Torque On-Chip Caches: A Device/Circuit/Systems Perspective. *IEEE Transactions on Magnetics*, **2014**, 50, 1-11	2	3
103	Scalable Effort Hardware Design. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 2004-2016	2.6	43
102	Design and management of hybrid electrical energy storage systems for regulation services **2014**,		10
101	ASLAN: Synthesis of approximate sequential circuits **2014**,		13
100	Attacking and Defending a Diabetes Therapy System **2014**, 175-193		8
99	Analysis and characterization of inherent application resilience for approximate computing **2013**,		284
98	ROBESim: A retrofit-oriented building energy simulator based on EnergyPlus. *Energy and Buildings*, **2013**, 66, 88-103	7	27
97	Localized Heating for Building Energy Efficiency **2013**,		3
96	Improving the Trustworthiness of Medical Device Software with Formal Verification Methods. *IEEE Embedded Systems Letters*, **2013**, 5, 50-53	1	25
95	Substitute-and-simplify: A unified design paradigm for approximate and quality configurable circuits **2013**,		83

94	Multi-level magnetic RAM using domain wall shift for energy-efficient, high-density caches **2013**,		19
93	Low-Power Digital Signal Processing Using Approximate Adders. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 124-137	2.5	401
92	Quality programmable vector processors for approximate computing **2013**,		162
91	MedMon: securing medical devices through wireless monitoring and anomaly detection. *IEEE Transactions on Biomedical Circuits and Systems*, **2013**, 7, 871-81	5.1	106
90	Approximate computing: An integrated hardware approach **2013**,		37
89	Emerging Frontiers in Embedded Security **2013**,		14
88	Energy-efficient and Secure Sensor Data Transmission Using Encompression **2013**,		15
87	Energy-efficient recognition and mining processor using scalable effort design **2013**,		7
86	Towards trustworthy medical devices and body area networks **2013**,		11
85	Relax-and-retime **2013**,		16
84	Managing the Quality vs. Efficiency Trade-off Using Dynamic Effort Scaling. *Transactions on Embedded Computing Systems*, **2013**, 12, 1-23	1.8	7
83	DWM-TAPESTRI - An energy efficient all-spin cache using domain wall shift based writes **2013**,		51
82	Variation-Aware Voltage Level Selection. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 925-936	2.6	5
81	CLIP: Circuit Level IC Protection Through Direct Injection of Process Variations. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 791-803	2.6	15
80	Tarazu. *Computer Architecture News*, **2012**, 40, 61-74		48
79	Future cache design using STT MRAMs for improved energy efficiency **2012**,		62
78	INVISIOS. *Transactions on Embedded Computing Systems*, **2012**, 11, 1-20	1.8	1
77	TapeCache **2012**,		98

76	PIC: Partitioned Iterative Convergence for Clusters **2012**,		3
75	A Trusted Virtual Machine in an Untrusted Management Environment. *IEEE Transactions on Services Computing*, **2012**, 5, 472-483	4.8	28
74	Tarazu **2012**,		104
73	Secure reconfiguration of software-defined radio. *Transactions on Embedded Computing Systems*, **2012**, 11, 1-22	1.8	2
72	Recovery-based design for variation-tolerant SoCs **2012**,		6
71	SALSA **2012**,		201
70	Guest EditorsVIntroduction: Green Buildings. *IEEE Design and Test of Computers*, **2012**, 29, 5-7		1
69	On Modeling and Evaluation of Logic Circuits under Timing Variations **2012**,		14
68	Automatic generation of software pipelines for heterogeneous parallel systems **2012**,		3
67	IMPACT: IMPrecise adders for low-power approximate computing **2011**,		204
66	Energy efficient many-core processor for recognition and mining using spin-based memory **2011**,		11
65	VESPA: Variability emulation for System-on-Chip performance analysis **2011**,		4
64	MACACO: Modeling and analysis of circuits for approximate computing **2011**,		128
63	Dynamic effort scaling **2011**,		37
62	A framework for defending embedded systems against software attacks. *Transactions on Embedded Computing Systems*, **2011**, 10, 1-23	1.8	1
61	MDR **2011**,		17
60	Design of voltage-scalable meta-functions for approximate computing **2011**,		118
59	Hijacking an insulin pump: Security attacks and defenses for a diabetes therapy system **2011**,		16

58	Best-effort semantic document search on GPUs **2010**,		16
57	Secure Virtual Machine Execution under an Untrusted Management OS **2010**,		41
56	Variation-Aware System-Level Power Analysis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1173-1184	2.6	4
55	Scalable effort hardware design **2010**,		114
54	Exploiting the forgiving nature of applications for scalable parallel execution **2010**,		10
53	An evaluation of energy-saving technologies for residential purposes **2010**,		8
52	Best-effort computing **2010**,		76
51	Best-effort parallel execution framework for Recognition and mining applications **2009**,		31
50	A framework for efficient and scalable execution of domain-specific templates on GPUs **2009**,		27
49	Variation-Tolerant Dynamic Power Management at the System-Level. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 1220-1232	2.6	10
48	Dynamically Configurable Bus Topologies for High-Performance On-Chip Communication. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2008**, 16, 1413-1426	2.6	13
47	Analysis and design of a hardware/software trusted platform module for embedded systems. *Transactions on Embedded Computing Systems*, **2008**, 8, 1-31	1.8	22
46	Systematic Software-Based Self-Test for Pipelined Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2008**, 16, 1441-1453	2.6	61
45	Dynamic Binary Instrumentation-Based Framework for Malware Defense. *Lecture Notes in Computer Science*, **2008**, 64-87	0.9	9
44	Configuration and Extension of Embedded Processors to Optimize IPSec Protocol Execution. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2007**, 15, 605-609	2.6	5
43	Automatic Power Modeling of Infrastructure IP for System-on-Chip Power Analysis **2007**,		9
42	Aiding Side-Channel Attacks on Cryptographic Software With Satisfiability-Based Analysis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2007**, 15, 465-470	2.6	12
41	. *IEEE Design and Test of Computers*, **2007**, 24, 518-520		5

40	Energy-optimizing source code transformations for operating system-driven embedded software. *Transactions on Embedded Computing Systems*, **2007**, 7, 1-26	1.8	16
39	Generation of Heterogeneous Distributed Architectures for Memory-Intensive Applications Through High-Level Synthesis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2007**, 15, 1191-1204	2.6	15
38	Hybrid Architectures for Efficient and Secure Face Authentication in Embedded Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2007**, 15, 296-308	2.6	5
37	Energy and Execution Time Analysis of a Software-based Trusted Platform Module **2007**,		11
36	Automated Energy/Performance Macromodeling of Embedded Software. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 542-552	2.5	10
35	Hybrid Simulation for Energy Estimation of Embedded Software. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 1843-1854	2.5	8
34	A Synthesis Methodology for Hybrid Custom Instruction and Coprocessor Generation for Extensible Processors. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 2035-2045	2.5	12
33	Architectural Support for Run-Time Validation of Program Data Properties. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2007**, 15, 546-559	2.6	12
32	A Framework for Extensible Processor Based MPSoC Design **2007**, 65-95		2
31	Software architecture exploration for high-performance security processing on a multiprocessor mobile SoC **2006**,		5
30	Architectural support for safe software execution on embedded processors **2006**,		10
29	Considering process variations during system-level power analysis **2006**,		9
28	Systematic software-based self-test for pipelined processors **2006**,		16
27	Hardware-Assisted Run-Time Monitoring for Secure Program Execution on Embedded Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2006**, 14, 1295-1308	2.6	46
26	A Scalable Synthesis Methodology for Application-Specific Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2006**, 14, 1175-1188	2.6	20
25	The LOTTERYBUS on-chip communication architecture. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2006**, 14, 596-608	2.6	28
24	Design of Communication Architectures for High-Performance and Energy-Efficient Systems-on-Chips **2005**, 187-222		3
23	Efficient fingerprint-based user authentication for embedded systems **2005**,		17

22	SECA **2005**,		39
21	Automated energy/performance macromodeling of embedded software **2004**,		16
20	Power analysis of system-level on-chip communication architectures **2004**,		29
19	Security in embedded systems. *Transactions on Embedded Computing Systems*, **2004**, 3, 461-491	1.8	266
18	Security as a new dimension in embedded system design **2004**,		57
17	Emerging Challenges in Designing Secure Mobile Appliances **2003**, 103-127		
16	Analyzing the energy consumption of security protocols **2003**,		81
15	High-level macro-modeling and estimation techniques for switching activity and power consumption. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2003**, 11, 538-557	2.6	18
14	System design methodologies for a wireless security processing platform. *Proceedings - Design Automation Conference*, **2002**,		14
13	Fast system-level power profiling for battery-efficient system design **2002**,		1
12	Synthesis of custom processors based on extensible platforms. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, **2002**,		31
11	Securing wireless data **2002**,		31
10	Cosimulation-based power estimation for system-on-chip design. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2002**, 10, 253-266	2.6	25
9	Battery life estimation of mobile embedded systems **2001**,		103
8	Power analysis of embedded operating systems **2000**,		46
7	Behavioral synthesis of fault secure controller/datapaths based on aliasing probability analysis. *IEEE Transactions on Computers*, **2000**, 49, 865-885	2.5	19
6	Power management in high-level synthesis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **1999**, 7, 7-15	2.6	17
5	Design for Testability Techniques at the Behavioral and Register-Transfer Levels. *Journal of Electronic Testing: Theory and Applications (JETTA)*, **1998**, 13, 79-91	0.7	1

List of Publications

4	Verification of RTL generated from scheduled behavior in a high-level synthesis flow **1998**,	10
3	Incorporating speculative execution into scheduling of control-flow intensive behavioral descriptions **1998**,	15
2	High-Level Power Analysis and Optimization **1998**,	103
1	Glitch analysis and reduction in register transfer level power optimization **1996**,	2